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MODEL 6401

Programmable Counter - Timer

(PREFIX 501)

Beckman

Operating and Servicing Manual

Electronic Instruments Division

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Programmable Counter - Timer

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DATA SERVICES

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JANUARY 1970
(REV. AUG. 1970)

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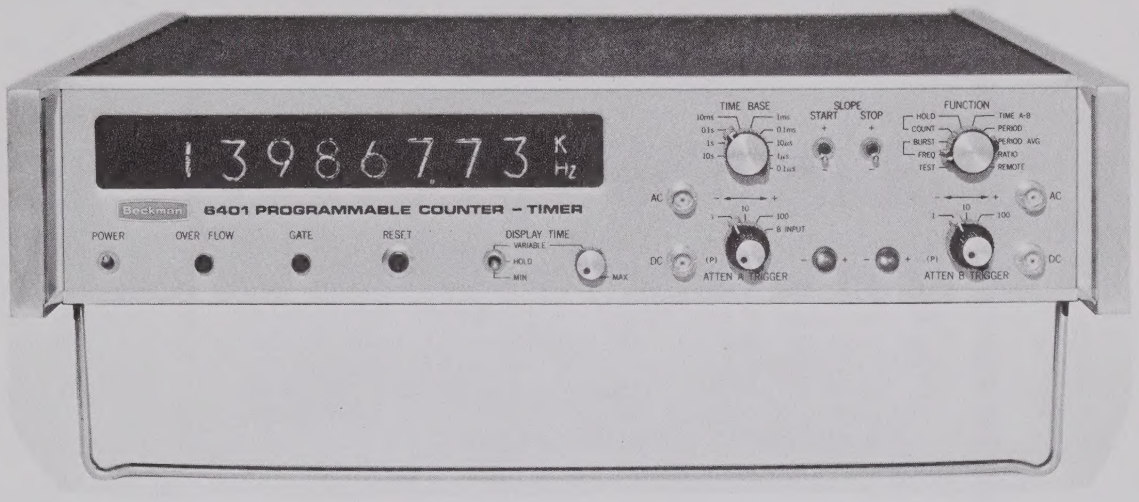

Model 6401 Programmable Counter-Timer

Frontispiece

MANUAL REVISIONS

Beckman Instruments is continually striving to provide better quality in its products. As a result, changes are initiated to improve performance and specifications.

Several changes may have been incorporated in your instrument since the manual was last printed. If this is the case, may we impose on you to make these changes to your copy of the manual? All changes are given in the form of addenda, one addendum for each change. They are printed on green-colored paper and inserted, in letter or number sequence, immediately following this page. If a change does not apply to your instrument, please disregard the associated addendum.

PREFIX NUMBERS

The prefix number denotes a generation of manuals. All addenda for a certain prefix number are incorporated in the manual before reprinting and the number increased by one (e.g., "Prefix 500" becomes "Prefix 501").

MODEL 6401

Addendum A

eco 12323
(10-70)

To bring the Input Board Component Layout (dwg. no. D437037-Rev. D) up revision level "E" (Page 5-5):

- change Z5 and Z7 to MC1027P Beckman Part No. 885-435202.
- change the parts list accordingly.
- change the schematic diagram, no. D437036-Rev. D to revision "E".

Addendum B

eco 12319
(10-70)

To bring the Count Board Component Layout (dwg. no. D437063-Rev. F) up to revision level "G" (Page 5-15):

- change resistors R2, 4, 6, 8, 10, 12, 14, 16, 22, 24, 26, 28, 30, 32, and 42 to 8.2K, 1/4W, 5% resistors, Beckman Part No. 601-822331.
- change the parts list accordingly.
- change the schematic diagram, no. D437062-Rev. E to revision "F".

Addendum C

ecr 1302
(10-70)

To bring the Oscillator Board Assembly (dwg. no. C437355-Rev. A) up to revision level "A-1" (Page 5-26):

- change Q5 to Beckman Part No. 755-822713; Mfr.: Texas Instruments 2N930,
- change Q6 to Beckman Part No. 755-857485; Mfr.: Texas Instruments TIS-58G,

continued. . .

Addendum C - cont'd

- delete R11 and R12; replaced with 1/4W Metal Film resistor, value to be selected in test.
- change the parts list on Page 5-27 accordingly, for the above.

Change the fuse, F2, (Basic Assembly Parts List, Page 5-25) to Beckman Part No. 731-029623; Mfr.: Bussman AGC 312.

Addendum D

Please note the following change on Page 5-12:

- Z4, 13, 19, 885-846625, should be: I. C., MC862P.

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SECTION 1
INTRODUCTION

1.1 GENERAL

The Beckman Model 6401 Programmable Counter-Timer measures frequency, period, multiple period, time interval, and frequency ratio through a frequency range of 0 to 136 MHz.

The instrument is supplied with one of three time base reference oscillator/multipliers. The difference in oscillator stability and aging rates determines the dash letter after the model number on the rear panel of the instrument. The three time bases are designated as Model numbers: 6401-O, 6401-L, and 6401-N.

The unit provides eight digits of inline numerical readout with automatically positioned decimal point and legend information. Additional features include remote programming of front-panel controls, BCD storage, BCD outputs, and trigger level monitor lamps. The instrument is constructed primarily of integrated circuits, all of which are mounted in sockets for ease of troubleshooting and repair.

The counter will accept a wide range of inputs. Three attenuator positions, AC-DC coupling and trigger level adjustments are provided for both input channels. The individual selection of start and stop slope polarity is provided for time interval and period measurements.

1.2 SPECIFICATIONS

Specifications for the Model 6401 are given in Table 1-1.

Table 1-1. Model 6401 (O, L, N) Specifications

Frequency	Channel A: 0 Hz to 136 MHz (dc input). 10 Hz to 136 MHz (ac input). Channel B: 0 Hz to 10 MHz (dc input). 10 Hz to 10 MHz (ac input).
Single Period (Channel A or B)	Resolution: 0.1 μsec to 10 sec in decade steps. Range: 0.1 μsec to 10^8 sec Std. Slope Selection: Start + or -. Stop + or -.
Period Average (Channel A or B)	Resolution: 0.1 μsec. Range: 0.1 μsec to 10^8 sec standard. Multiplier Range: 1 to 10^8 in decade steps.
Time Interval (Time A to B)	Resolution: 0.1 μsec to 10 sec in decade steps. Range: 0.1 μsec to 10^8 sec Std. Slope Selection: Start + or -. Stop + or -.

continued. . .

Table 1-1. Model 6401 (O, L, N) Specifications - continued

Ratio $\frac{\text{Freq A}}{\text{Freq B}} \times N$	Frequency Range A: 0 Hz to 136 MHz (dc input). 10 Hz to 136 MHz (ac input). Frequency Range B: 0 Hz to 10 MHz (dc input). 10 Hz to 10 MHz (ac input). Range Multiplier N: 1 to 10^8 in decade steps.
Count/Hold	Count random pulses. Channel Range A: 0 to 136×10^6 pulses per sec. Channel Range B: 0 to 10×10^6 pulses per sec.
Input Characteristics (Channels A and B)	Attenuation Factors: 1 / 10 / 100 Sensitivity (rms): 0.1 V / 1.0 V / 10 V Resistance (dc): 1.0 MΩ / 1.0 MΩ / 1.0 MΩ Trigger Level: ±1.0 V / ±10 V / ±100 V DC Overload: 150 V / 500 V / 500 V DC Blocking: 500 V / 500 V / 500 V
Coupling	AC or DC.
Input Capacitance	Input resistance shunted by less than 25 pF.
Trigger Slopes	Positive or negative for start and stop.
Internal Reference Frequency	10 MHz.
Oscillator Specifications	Model 6401-O: Aging Rate: 3 parts in 10^{-9} per 24 hours averaged over 30 days and 1 part in 10^{-6} per year. Temperature: 1.5 parts in 10^{-6} from 0°C to 50°C. Line Voltage: 2 parts in 10^{-8} for ±10% line changes. Warm Up: 2 minutes to achieve 1 part in 10^{-6} of final value. Model 6401-L: Replaces standard time base oscillator with laboratory stability oscillator, 3 parts in 10^9 per 24 hours. Model 6401-N: Replaces standard time base oscillator with an ultra-high stability oscillator, fast warm-up, 5 parts in 10^{10} per 24 hours.
Accuracy	a) Frequency: ±1 count ± oscillator stability. b) Single Period: ±1 count ± oscillator stability ± trigger error. c) Multiple Period: ±1 count ± oscillator stability $\pm\frac{\text{trigger error}}{\text{periods averaged}}$. For 0.1 V rms sine wave with a signal-to-noise ratio ≤ 40 dB. Trigger error ≤ 0.3% of one period.

continued. . .

Table 1-1. Model 6401 (O, L, N) Specifications - continued

Display	a) Eight inline digits are displayed on numerical glow tubes. Display includes automatically-positioned decimal point. The legend displayed is KHz and MHz for frequency measurements, and μS, mS, S, and KS for time interval measurements. b) Storage On: Display is updated at the completion of a measurement. c) Storage Off: Display follows the counting process.
Display Time (Minimum time between measurements)	Continuously variable from 0.1 to 10 sec. in VARIABLE mode. Nominal 40 μsec in MIN mode and infinite in HOLD mode.
Coded Output	a) Four-line, 1-2-4-8 BCD output at rear panel (Amphenol 40500, 50-pin connector). Binary 0 is 0 V to +0.5 V, binary 1 is +4 V to +5 V. b) Data is available from buffer storage in all modes except Count or Storage Off in which the data is continuously updated. c) Print command is a logical 1 with a nominal 10 μsec duration.
Auxiliary Inputs	a) External Reference: Accepts external frequencies of 1, 2.5, or 5 MHz as a substitute for internal reference; 1000Ω input resistance. Voltage requirements at each frequency are: 1 MHz - from 0.5 V p-p to 6 V p-p. 2.5 MHz - from 0.5 V p-p to 6 V p-p. 5 MHz - from 0.5 V p-p to 1 V p-p. b) Inhibit: Contact closure to ground or logic 0 which must occur before end-of-print command. Logic 0 is 0 V to +0.5 V. c) Reset: Contact closure to ground or 0 V to +0.25 V, logic 0. 1 μsec minimum pulse duration.
Auxiliary Outputs	Oscillator Output: 10 MHz, 2.8 V p-p pulse, 50% duty cycle. Time Base Output: Logic 1 for a duration of 100 ns from a 300Ω source. Logic 0 is 0 V to +0.5 V; logic 1 is +3.5 V to +5 V. Gate Marker Output: A negative pulse, 400 ns ±50% duration at 50% amplitude. Logic 0 is +15 V with a 2.7 K nominal source resistance. Logic 1 is a saturated transistor with 0 to +0.5 V with a load current of 10 mA or less. The gate marker outputs are suitable for intensity modulation of standard laboratory oscilloscopes.
Power	115 V or 230 V (selectable at rear panel). 50 to 60 Hz. 63 Watts maximum.
Temperature	Operating: 0 to +55°C. Storage: -55°C to +75°C.
Weight	20 pounds.
Dimensions	3.5 in. high; 17 in. wide; 18.5 in. deep.

1.3 OPTIONS & ACCESSORIES

Options and accessories available for the Model 6401 are shown in Table 1-2. Detailed information, including diagrams and parts lists, are given in Section 6 at the rear of this manual. For specific requirements contact the factory direct or a Beckman Sales Representative.

1.4 AUXILIARY EQUIPMENT

Auxiliary equipment includes printers, oscilloscopes, signal generators, and other signal recording and source instruments. See Section 2 (paragraph 2.8, Using a Digital Recorder, and Table 2-6) for connection requirements for this type of equipment.

Table 1-2. Options and Accessories*

	Options
C9	Adds 9th in-line digit. Maximum display number before overflow is 999,999,999.
C11	Input Attenuator and AC/DC select are remotely programmable functions
	Accessories
RM1	Rack ears for 19-inch rack.
RM2	Rack slides, including rack ears.

* For detailed information, refer to Section 6 at the rear of this manual.

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SECTION 2
INSTALLATION & OPERATION

2.1 UNPACKING & HANDLING

Before shipment, the instrument is thoroughly tested and inspected, then carefully packed. The unit should be unpacked with the care due any precision instrument. If the packing case shows signs of damage, make a note to this effect on the freight receipt.

Remove packing carton and braces, being careful not to scar or damage the unit. Make a complete visual inspection of the equipment; check for damage or missing components. Check that all switches and controls operate mechanically. Report any damage immediately to Beckman Instruments, Inc. by calling (415) 526-7730, and ask for Shipping Department. Avoid storing the units in extreme conditions of temperature or humidity (beyond the range of $-55^{o}C$ to $+75^{o}C$).

2.1.1 Reshipping

Should it become necessary to return the unit to the factory for any reason, follow these packing instructions:

1) Wrap the unit in polyethylene sheeting, sealing all sides.
2) Punch small air holes in the sheeting.
3) Wrap the unit with rubberized hair and pack in carton.
4) Seal the carton and mark it clearly: "FRAGILE — Handle with Care."

2.2 INSTALLING THE UNITS

The Counter-Timer is portable or rack-mounted. No special installation requirements are necessary unless peripheral equipment, such as printers and oscilloscopes, are used. In these cases the instrument should be located as close as possible to support equipment.

Rack ears are supplied with the rack-mounted version of the instruments. Integral rack slides can be ordered as an option. If slides are ordered, mount on rack, being careful that instrument clears other equipment when moved in and out of the rack.

2.2.1 Applying Power

Determine whether 115 or 230 volt ac power is available, and set rear-panel LINE switch accordingly. Plug power connector into power source. With Model 6401-L or 6401-N, crystal oscillator and oven are energized immediately. These oscillators require approximately one hour to warm up.

2.3 OPERATION

Two basic signal sources drive the instrument. Input signals applied to the A and B Channel circuits at the front panel provide start, stop, and count signals, depending on operating mode. An internal time base generator also supplies start, stop, and count signals depending on operating mode. Start signals open the count gate, stop signals close the count gate, and count signals pass through the open gate for accumulation and display on the front-panel readout. With appropriate signal combinations, the instrument measures frequency, period, time interval, and ratio.

Prepare to operate the Counter-Timer by first reading the following sections on controls, accuracy, and applying input signals. Optimum

use of this equipment requires an understanding of its operating features and limitations.

2.3.1 Controls and Indicators

Table 2-1 describes the front-panel controls and indicators illustrated in Figure 2-1. Table 2-2 describes the controls on the rear panel, illustrated in Figure 2-2. Once rear-panel controls are set, the instrument can be operated entirely from the front panel or by remote electrical control. Refer to Table 1-1 for specific parameters relating to each control.

Table 2-1. Front-Panel Controls and Indicators

Control or Indicator	Function
POWER Switch	Turns on power to all circuits. (With Models 6401-L or -N, oven and oscillator power are on when ac power is applied to the instrument.)
TIME BASE and FUNCTION Switch(es)	Selects time base for FREQ and BURST functions, time interval (TIME A-B), and single PERIOD modes. Selects multiplier for PERIOD AVG and RATIO average modes.
ATTEN A TRIGGER Switch	Selects attenuation factor for signals applied to A Channel. Selects B input for single input measurement functions.
TRIGGER Control	Adjusts point along A input voltage excursion that fires input Schmitt trigger.
TRIGGER Light	Indicates zero level trigger setting.
AC-DC Input Connectors	Couples A input signal to A channel attenuator. AC connector is capacitively coupled, DC connector is direct coupled.
ATTEN B TRIGGER Switch	Selects attenuation factor for signals applied to B channel.
TRIGGER Control	Adjusts point along B input voltage excursion that fires input Schmitt trigger.
TRIGGER Light	Indicates zero level trigger setting.
AC-DC Input Connectors	Couples B input signal to B channel attenuator. AC connector is capacitively coupled, DC connector is direct coupled.
RESET Pushbutton	Provides manual reset of all functions.
OVERFLOW Light	Indicates when count exceeds the accumulator capacity.
GATE Light	Indicates when gate is open.
DISPLAY TIME Control Switch(es)	Switch selects VARIABLE, HOLD, and MIN (fast recycle) modes. Knob adjusts recycle time when in VARIABLE mode.
SLOPE START/STOP Switches	Determine which slope of input signal starts and stops counting. (Used in PERIOD, TIME A-B and RATIO modes.)

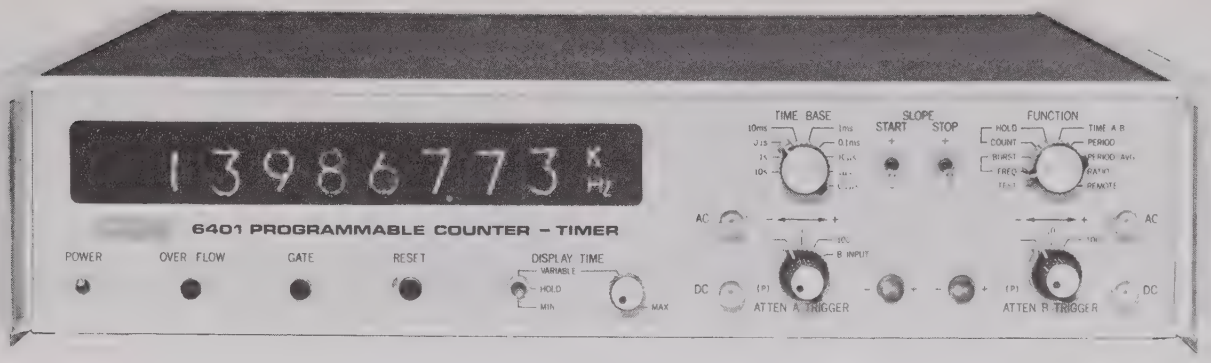

Figure 2-1. Front-Panel Controls and Indicators

Table 2-2. Rear-Panel Controls and Connectors

Control or Connector	Function
DIGITAL RECORDER Connector	Provides four-line 1-2-4-8 BCD output. (See paragraph 2.8 for details.)
OSC ADJ	Adjusts oscillator frequency.
OSC OUT - REF FREQ INPUT Switch	Selects internal or external reference frequency.
OSC OUT - REF FREQ INPUT Connector	Couples internal reference frequency out or external reference frequency in. CAUTION Do not apply external signal when switch is in OSC OUT position.
START Connector	Provides pulse output to mark count gate opening.
STOP Connector	Provides pulse output to mark count gate closure.
STORAGE ON-OFF Switch	Enables or disables the data storage registers.
TIME BASE Connector	Provides time base signal output.
REMOTE Connector	Provides remote operation. (See paragraph 2.7 for details.)
LINE Switch	Selects power supply transformer connections for 115 V or 230 V ac, depending upon power input voltage.
F1 Fuse	Provides overload protection for oscillators and ovens for Models 6401-L and 6401-N.
F2 Fuse	Provides overload protection for counter.

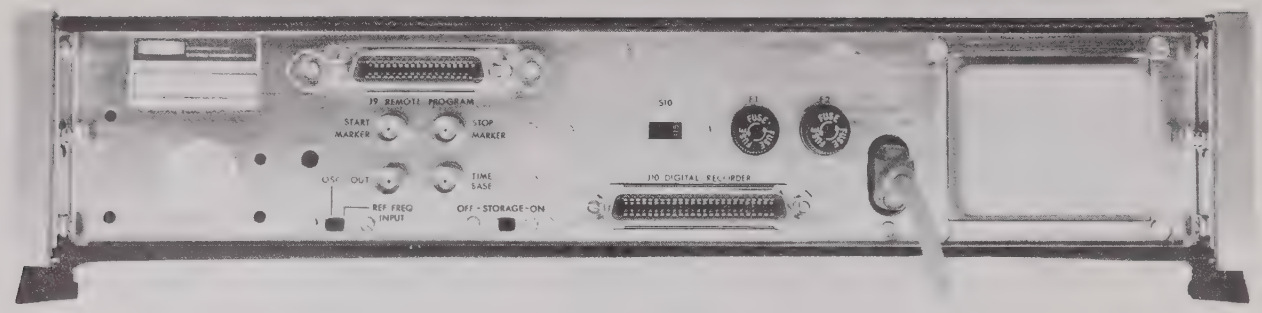

Figure 2-2. Rear-Panel Controls

2.3.2 Readout and DISPLAY TIME Control

The STORAGE switch is used to enable and disable the data storage. When in the OFF position, the readout displays each accumulated count as it is counted. When in the ON position, the data is stored in a register which is updated at the end of each measurement. When COUNT and HOLD modes are used, the storage function is internally disabled.

The DISPLAY TIME control determines the time from the end of one measurement to the resetting of the instrument for another measurement. With storage off, it is the display time, for the reset returns the display to zero. With storage on, it essentially determines the time between readings.

With the DISPLAY TIME switch in the VARIABLE position, the time is determined by the adjustment knob. In this mode, control range is 0.1 second to 10 seconds.

When in HOLD mode, a measurement is stored until a manual or external reset occurs. When in the MIN mode, the display time is fixed at less than 40 microseconds.

2.4 ACCURACY

Three basic factors affect measurement accuracy of any counter of this type: gating error, oscillator stability, and input noise. Some error factors can be minimized by proper instrument settings.

2.4.1 Gating Error

Gating action produces error no more than ± 1 count. If the gate opens just before one count pulse and closes immediately after another, the front panel indication may be one time unit high. If the gate opens just after a pulse and closes just before another, the indication may be one unit low. For TIME A-B and PERIOD measurements, this error is very slight if the time units selected are small compared to the interval being timed.

2.4.2 Oscillator Stability

Although oscillator stability is high, small frequency deviations occur between calibrations. Once set, the oscillator does not vary more than 2 parts in 10^8 per week (assuming standard unit). Measurements made within the same week have a comparative maximum error of 0.000002%. If absolute time is important, adjust the oscillator (see Section 4) to correspond with the standard frequencies broadcast from the National Bureau of Standards radio stations WWV, WWVH, or WWVB (Fort Collins, Colorado).

2.4.3 Input Noise

Input noise (defined as any voltage variation not representative of the event being timed) can cause the input voltage to reach the count trigger too soon. As shown in Figure 2-3, the counter sees an event before the event of interest passes through the input trigger level. This type of error is minimized by obtaining the greatest possible signal-to-noise ratio, and by reducing input rise time. Figure 2-4 illustrates decreased error when using a faster rising signal.

If needed, the actual error can be calculated. Letting t = maximum error in seconds, E_n = peak-to-peak noise in volts, and S = slope of input signal at trigger point in volts/second, the error t is:

$$t = \frac{E_n}{S} .$$

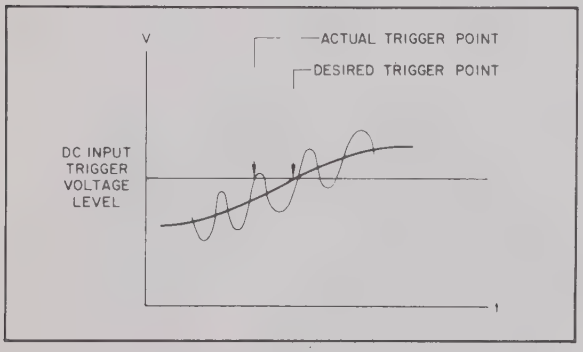

Figure 2-3. Error Due to Noise

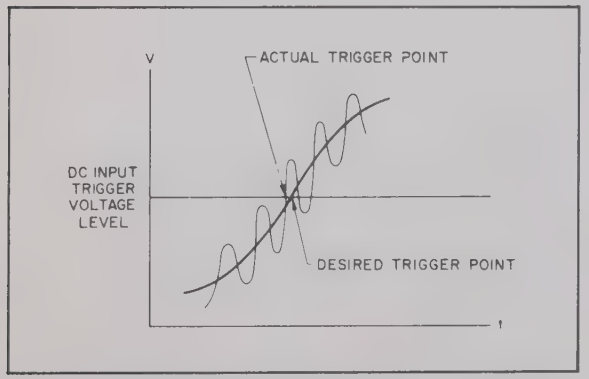

Figure 2-4. Reducing Error Due to Noise By Increasing Rise Time

2.5 OPERATING PROCEDURES

2.5.1 Adjusting Input Circuits

Because the Counter-Timer is basically a digital instrument, the wide variety of input signals accepted by the unit must be conditioned for waveform and voltage level before entering the counting circuits. The TRIGGER, ATTEN, and INPUT controls set the conditioning parameters for the A and B Channel inputs.

The two INPUT connectors for each channel provide either AC or DC coupling of the input signal. Choice of coupling mode depends upon dc component and frequency of input.

2.5.2 ATTEN Switch

Attenuation of the input voltage brings the signal within working range of the TRIGGER control. This switch selects the appropriate attenuation factor for a given input. When using this control, remember the following rules:

a) Attenuating the input signal reduces the absolute value of the slope at all points.

b) Attenuating the input signal shifts the ac component nearer ground if it rides on a dc level.

c) Attenuating a noisy signal reduces the influence of noise on the trigger circuit.

d) The attenuated signal should be no more than 2 volts peak-to-peak to assure optimum use of the TRIGGER control.

2.5.3 TRIGGER Control

The sensitivity of the input trigger circuit depends on a small hysteresis range centered about a fixed dc voltage at the trigger input. As shown in Figure 2-5, a rising voltage excursion must pass through the hysteresis upper limit to

start an output pulse, while the falling slope must pass through the lower limit to stop the pulse. The TRIGGER control varies the dc component of the attenuated input by ±1 volt, in effect shifting the points along the input voltage excursion that trip the Schmitt trigger. It is desirable to be able to choose any point along this excursion as the trigger point. This means attenuated signals should not exceed two volts peak-to-peak.

Figure 2-6 shows a signal too large for the ±1 volt range of the TRIGGER control. Attenuating this signal further gives the signal shown in Figure 2-7. It can be shifted outside the hysteresis range on either side, providing maximum operating flexibility.

A preset position is provided which places this trigger level at 0 volts for convenient triggering on waveforms which cross the zero voltage point. DC components can be removed by using the ac input.

2.5.4 TRIGGER Lights

Each input channel has a small TRIGGER indicator light with two lamps. The lamps indicate the state of the input Schmitt trigger. At any given point of time, one lamp is on, the other off. As shown in Figure 2-8, the lamps alternate when the trigger circuit changes states. This provides a precise means of adjusting the TRIGGER control. Note that the TRIGGER lights may not be meaningful above 5 MHz in PERIOD or TIME A-B modes.

For fast signals, the lamps switch faster than can be detected by the human eye. However, the light that is on the most will seem brighter, and the point at which triggering starts and stops can usually be found.

A great deal can be learned about the input signal from the TRIGGER lights.

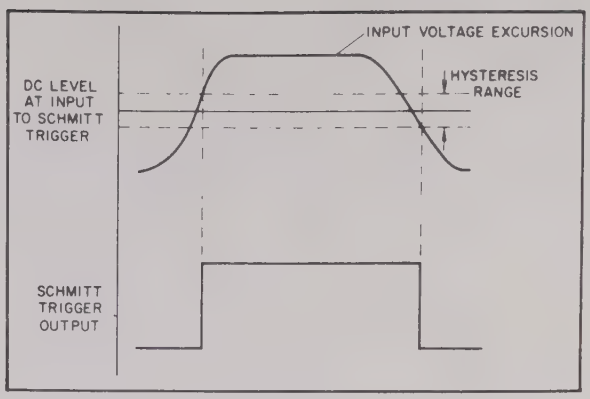

Figure 2-5. Trigger Output

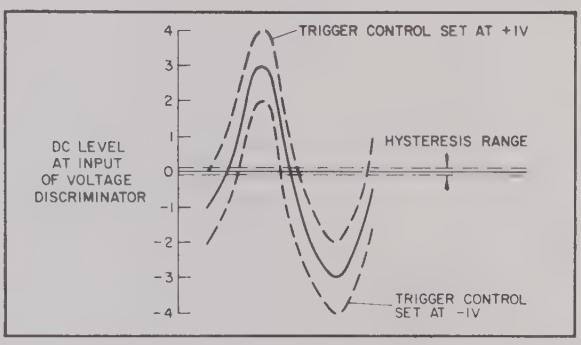

Figure 2-6. Voltage Excursion too Great for Trigger Control

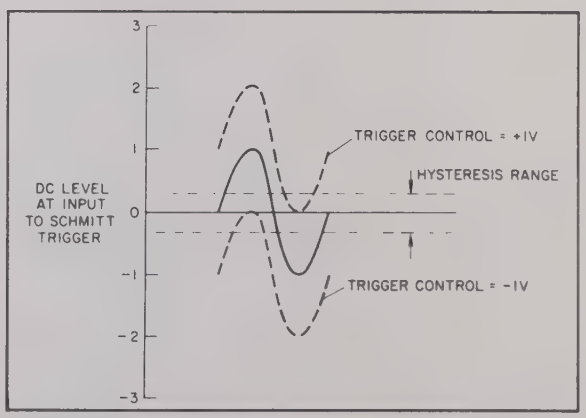

Figure 2-7. Voltage Excursion Attenuated for Trigger Control

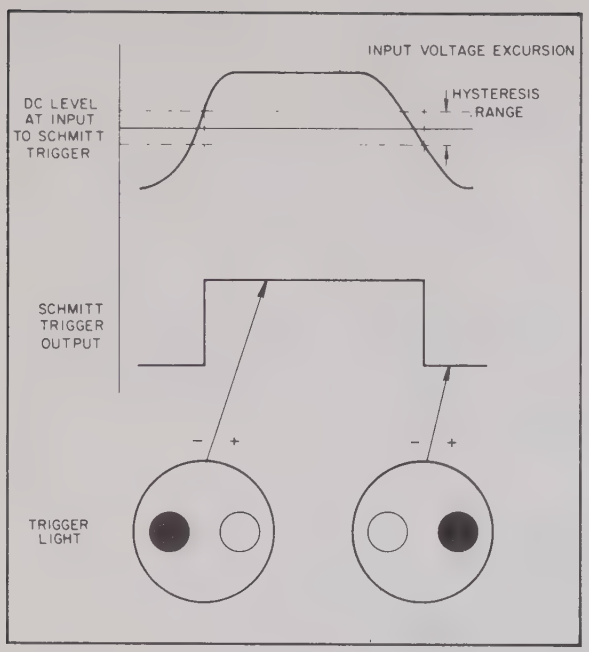

Figure 2-8. Operation of Trigger Light

a) If both lights stay on throughout the range of the TRIGGER control, the input peak-to peak signal level is too high. This calls for more attenuation.

b) If one light stays on and the other off throughout the range of the TRIGGER control, no triggering occurs. This usually means that the dc component of the input signal is too high, and indicates the need for ac coupling.

c) For symmetrical and periodic signal, if the two lamps cannot be made equally bright, the attenuated signal is too weak.

d) The TRIGGER light provides a shortcut method of adjusting the TRIGGER control. This method only applies to signals having both negative and positive voltage levels.

- With no input connected, locate the two points on the TRIGGER control that flip the Schmitt trigger. These points are indicated when TRIGGER light switches.
- Set TRIGGER control midway between these points. This establishes a 0 dc voltage level at the input of the Schmitt trigger.
- Connect input signal to AC connector and find ATTEN factor that gives smooth counting.

2.5.5 SLOPE Switches

The SLOPE switches determine which slope of the input signal starts and stops counting when the instrument measures period, time interval and ratio.

2.5.6 Adjusting A Channel Input

Both preset and variable trigger levels are provided. The preset trigger level is appropriate for general trigger requirements. For signals with dc bias, the ac input will remove the bias component. The variable trigger control is for achieving specific triggering conditions for peculiar waveforms or noisy waveforms.

NOTE

These instructions presuppose little prior knowledge regarding the input signal. In most circumstances, however, the operator knows enough about the signal to make fairly accurate preliminary adjustments.

2.5.7 Adjustment Procedure - Preset Trigger Level

a) Connect input signal to AC connector.

b) Set A ATTEN switch to 100.

c) Turn POWER switch to ON.

d) Set A TRIGGER control to (P) preset position.

e) If no counting occurs, change A ATTEN switch to 10.

f) If no counting occurs, change A ATTEN switch to 1.

g) If no counting occurs, check that the input signal is at least 0.1 V rms or 300 mV peak-to-peak. If not, insert appropriate amplifier between signal source and counter.

2.5.8 Adjustment Procedure - Variable Trigger Level

a) Connect input signal to DC connector.

b) Set A ATTEN switch to 100.

c) Turn POWER switch to ON.

d) Turn FUNCTION switch to HOLD, press RESET button to clear instrument, and then turn FUNCTION switch to COUNT.

e) Slowly turn A TRIGGER control between its extreme positions and note whether counting occurs. If counting occurs, proceed to step g. Otherwise continue to step f.

f) Reduce ATTEN factor until counting occurs. If no counting occurs, connect input to AC connector, begin with an ATTEN factor of 100, and repeat above procedure until counting occurs. If no counting occurs after this, check that input signal has an rms value of at least 0.1 volt. If not, insert appropriate amplifier between signal source and counter.

g) Final adjustment of A TRIGGER and A ATTEN control can be accomplished with three techniques: observing count for rough adjustment, observing TRIGGER light for fine adjustment, and using an oscilloscope for highly accurate adjustment. In general, fine adjustment is sufficient.

- Observing Count. Move the TRIGGER control through its full range and note the points at which counting starts and stops. Place TRIGGER control midway between these points. If circuit is triggering properly, the change of count on readout is smooth. If circuit is not triggering properly, count appears to jump and jitter.

- Observing TRIGGER Light. If input signal is periodic and symmetrical, adjust TRIGGER control until both lamps are equally bright. Make sure that turning TRIGGER control changes this balance. See paragraph 2.5.4 for interpreting other TRIGGER light indications and using TRIGGER light for short-cut adjustment.

- Oscilloscope. An oscilloscope can be used when the above methods fail to give proper triggering. Check START and STOP markers on rear panel to determine exact trigger points, then set TRIGGER control midway between these points. For greater accuracy, check input signal with oscilloscope for level and waveform, then set A INPUT controls accordingly.

2.5.9 Adjusting B Channel Input

Set the A Channel attenuator switch to B INPUT position. Use the procedure outlined in paragraph 2.5.6.

2.6 OPERATION - MANUAL CONTROL

The following paragraphs give step-by-step instructions for operating the instrument using manual control.

Prior to operation, set the rear-panel controls as follows:

a) Make sure LINE switch is set for proper line voltage.

b) Set STORAGE switch to ON.

NOTE

To avoid improper operation, never set OSC OUT - REF FREQ INPUT switch to OSC OUT with external frequency connected to OSC OUT jack.

c) Set OSC OUT - REF FREQ INPUT switch to OSC OUT if no external reference frequency is used.

IMPORTANT NOTE

Invalid Combination of Control Setting

When using the TEST, FREQ, and BURST functions on the FUNCTION switch, the TIME BASE switch setting of .1 μs is invalid.

2.6.1 TEST Mode

The TEST mode is performed by routing the reference frequency to the time base divider and to the gate. The time base divider divides the reference frequency by 10^0 to 10^8, determined

by the front-panel TIME BASE selector switch or REMOTE program. The displayed function is:

10^n counts, where n = 0 to 8 determined by the time base selected.

$\frac{\text{Input Frequency}}{\text{Reference Frequency}} \times 10^n$ counts,

where n is determined by the TIME BASE selector switch or REMOTE program.

The channel output routed to the gate is selected by the A channel attenuator switch on the front panel or by REMOTE program.

To perform TEST mode:

1) Turn POWER switch to ON position.

2) Turn DISPLAY TIME switch to VARIABLE and control knob fully counterclockwise.

3) Turn FUNCTION switch to TEST.

4) Set TIME BASE switch to 1 μs and observe display. It should correspond to the reading given in Table 2-3 for a 1 μs TIME BASE switch setting. Check each TIME BASE switch position from 1 μs to 10 s, verifying each reading.

Table 2-3. Test Indication

Time Base	Reading	Unit
1 μs	00000010.	MHz
10 μs	0000010.0	MHz
0.1 ms	000010.00	MHz
1 ms	00010000.	kHz
10 ms	0010000.0	kHz
0.1 s	010000.00	kHz
1 s	10000.000	kHz
10 s	0000.0000 plus OVERFLOW Lamp	kHz

2.6.2 FREQ Mode

The FREQ mode is performed in the same manner as the TEST mode, except that the output of the shaper from one of the input channels is routed to the gate in place of the reference frequency. The displayed function is:

$\frac{\text{Input Frequency}}{\text{Reference Frequency}} \times 10^n$ counts,

where n is determined by the TIME BASE selector switch or REMOTE program.

The channel output routed to the gate is selected by the A channel attenuator switch on the front panel or by REMOTE program.

To perform FREQ Measurement:

1) Turn POWER switch to the ON position.

2) Connect signal to A INPUT. Set ATTEN A switch to 100 and adjust inputs controls according to paragraph 2.5.6.

OR

Connect signal to B INPUT. Set ATTEN A switch to B INPUT position. Set ATTEN B to 100 and adjust according to paragraph 2.5.6.

3) Turn FUNCTION switch to FREQ.

4) Set TIME BASE switch to gate time appropriate to the input signal. In general, a greater time base increases the number of significant digits displayed, and hence increases resolution. Smaller gate times are usually used for higher frequencies. If the approximate frequency of the input signal is unknown, begin with a small gate period and change the TIME BASE switch until desired resolution is achieved.

5) Adjust DISPLAY TIME control for convenient reading or recording rate.

6) Readout gives direct indication of frequency, including decimal position and measurement unit.

2.6.3 BURST Mode

The BURST mode is performed in the same manner as the FREQ mode with the exception that the time base divider is disabled until the envelope of a carrier frequency is detected on the selected channel and the BURST control is enabled. This synchronizes the gate with the leading edge of a pulse modulated carrier, etc. Channel selection is accomplished with the A channel ATTEN switch or by REMOTE program.

The measurement procedure is the same as described in paragraph 2.6.2 under "FREQ Mode".

NOTE

The TIME BASE switch setting must be set at a time less than the duration of the carrier envelope to measure the frequency. If the duration of the envelope is not known, start with the 1 μs setting and observe the reading. If no reading occurs, switch to the next largest setting until a reading is obtained.

Continue to increase the TIME BASE setting until the readout does not increase by a factor of ten (10). Then reduce the TIME BASE switch setting by one position. The gate light will indicate its bursts are being detected.

The burst repetition rate can interact with the recycle time of the counter. It is best to set the DISPLAY TIME switch in the MIN position. This will allow measurements of burst repetition rates up to approximately 40 kHz with carrier frequencies up to 136 MHz on Channel A and 10 MHz on Channel B.

2.6.4 COUNT-HOLD Modes

The COUNT-HOLD functions are used for straight accumulation of events. The storage is disabled, and the shaper from the selected channel is routed to the gate. The gate is controlled by the selection of COUNT or HOLD. A reset is obtained only by manual or remote reset command. Channel selection is accomplished with the A channel ATTEN switch or by REMOTE program.

To perform random accumulation:

1) Turn POWER switch to ON position.

2) Connect signal to A Input. Set ATTEN A switch to 100 and adjust input controls according to paragraph 2.5.6.

   OR

   Connect signal to B Input. Set ATTEN A switch to B INPUT position. Set ATTEN B switch to 100 and adjust according to paragraph 2.5.6.

3) Turn FUNCTION switch to HOLD.

4) Push RESET button. This clears all storage registers and prepares circuits to begin counting.

5) Turn FUNCTION switch to COUNT. This opens count gate and begins data accumulation. To stop counting, turn FUNCTION switch back to HOLD.

NOTE

The maximum number of events which can be registered is 99,999,999. If the count gate stays open after this number is reached, the OVERFLOW indicator on the display panel lights. Counting will continue, with the readout starting at 0 once again. The OVERFLOW light will remain on until the RESET button is pressed (or the unit automatically resets in some other mode).

6) To start another count cycle, push RESET button and turn FUNCTION switch back to COUNT. To continue counting from the point held on the readout, turn FUNCTION switch to COUNT without pushing RESET button.

7) Readout does not include measurement unit or decimal point.

2.6.5 TIME A-B (Time Interval Measurement)

This mode programs the time mode selector circuits to route the A channel shaper to initiate counting by opening the gate; and the B channel shaper to terminate the counting by closing the gate. The reference frequency is routed to the time base divider where it is divided by 10^0 to 10^8. The output of the time base divider is routed to the gate to be counted for the gate duration. The resolution of the measurement is:

$$\frac{10^n}{\text{Reference Frequency}}$$

where n is determined by the TIME BASE selector switch or REMOTE program.

To perform TIME A-B measurement:

1) Turn POWER switch to the ON position.

2) Connect inputs to A INPUT and B INPUT and adjust controls according to paragraph 2.5.6.

3) Turn FUNCTION switch to TIME A-B.

4) Set SLOPE switches as desired. If START SLOPE is set to '+', the width of the event at A INPUT will be included in the time measurement; if set to '-', it will not be included. Setting STOP SLOPE switch to '-' causes B INPUT event to be included in measurement; setting it to '+' does not. The above assumes both events are positive going.

5) The TIME BASE switch determines the unit of measurement. Set this switch for a convenient time unit. In general, smaller time units give greater resolution.

6) Adjust DISPLAY TIME control for a convenient reading or recording rate.

7) Readout gives direct indication of count, unit of measurement and decimal point.

2.6.6 PERIOD Mode

This mode is the same as TIME A-B except that the time mode selector circuits route only the selected input channel to control the gate; i.e., with channel A selected, the channel A shaper will control both the opening and closing of the gate. The input channel is selected by the A channel attenuator switch or REMOTE program.

To perform PERIOD measurement:

1) Turn POWER switch to the ON position.

2) Connect input signal to A INPUT and adjust B INPUT controls according to paragraph 2.5.6.

3) Set SLOPE switches as follows:

- To measure the period of a periodic waveform, set both SLOPE switches to '+' or both to '-'.
- To measure the width of a positive waveform, set START SLOPE switch to '+' and STOP SLOPE switch to '-'.
- To measure the width of a negative waveform, set START SLOPE switch to '-' and STOP SLOPE switch to '+'.
- To measure separation of positive pulses, set START SLOPE switch to '-' and STOP SLOPE switch to '+'. Use reverse settings for negative pulses.

4) The TIME BASE switch determines the unit of measurement. Set this switch for a convenient time unit. In general, smaller time units give greater resolution.

5) Adjust DISPLAY TIME control for a convenient reading or recording rate.

6) Readout gives direct indication of count, unit of measurement and decimal point.

2.6.7 PERIOD AVG Mode

This mode is similar to the PERIOD mode except the closing of the gate is delayed by the time base divider. The gate is not closed until 10^0 to 10^8 stop functions have occurred. Resolution of the measurement is 0.1 microsecond divided by 10^0 to 10^8. The factor 0 to 8 is determined by the position of the TIME BASE selector switch or by REMOTE program.

To perform PERIOD AVG measurement:

1) Turn POWER switch to ON.

2) Connect input signal to A INPUT and adjust B INPUT controls according to paragraph 2.5.6.

3) Set SLOPE switches as follows:

- To measure the period of a periodic waveform, set both SLOPE switches to '+' or both to '-'.
- To measure the width of a positive waveform, set START SLOPE switch to '+' and STOP SLOPE switch to '-'.
- To measure the width of a negative waveform, set START SLOPE switch to '-' and STOP SLOPE switch to '+'.
- To measure separation of positive pulses, set START SLOPE switch to '-' and STOP SLOPE switch to '+'. Use reverse settings for negative pulses.

4) The counted frequency is fixed at 10 MHz. The TIME BASE switch selects the number of periods to be averaged. The relation of multiplier to TIME BASE switch setting is indicated in Table 2-4.

Table 2-4. Multiplier Setting

Time Base	Multiplier
0.1 μs	x 1
1 μs	x 10
0.1 ms	x 10^2
1 ms	x 10^3
10 ms	x 10^4
0.1 s	x 10^5
1 s	x 10^6
10 s	x 10^7

5) Adjust DISPLAY TIME control for a convenient reading or recording rate.

6) Readout gives direct indication of count, unit of measurement and decimal point.

2.6.8 RATIO Mode

This mode is a combination of FREQ A channel and PERIOD AVG B channel. The A channel shaper output is routed to the gate. The B channel shaper is selected to control the gate as described under "PERIOD AVG Mode." The displayed function is:

$$\frac{\text{Frequency Channel A}}{\text{Frequency Channel B}} \times 10^n$$

where n is 0 to 8 determined by the TIME BASE selector switch or REMOTE program.

To perform RATIO measurement:

1) Turn POWER switch to the ON position.

2) Connect higher frequency to A INPUT and adjust A INPUT controls according to paragraph 2.5.6.

3) Connect lower frequency to B INPUT and adjust B INPUT controls according to paragraph 2.5.9.

4) Set FUNCTION switch to RATIO.

5) Set the multiplier with the TIME BASE switch according to Table 2-4.

6) Adjust DISPLAY TIME control for a convenient reading or recording rate.

7) Readout gives a direct indication of the FREQ A/FREQ B ratio. The measurement is dimensionless and the decimal point gives the true ratio regardless of multiplier setting.

2.7 OPERATION - REMOTE CONTROL

The Counter-Timer can be operated by remote controls. All of the operations described in paragraphs 2.6 through 2.6.9 can be performed, with the exception of adjusting the ATTEN A and ATTEN B switches, and the selection of an AC or DC coupling. (The C11 option provides remote control of the ATTEN A and ATTEN B switches and AC or DC coupling.)

To operate with remote control, set the manual controls as follows:

1) Set the DISPLAY TIME switch to HOLD.

2) Set the A Channel and B Channel TRIGGER Level controls to (P) preset position.

3) Set the FUNCTION switch to REMOTE.

4) Set the STORAGE ON-OFF switch to ON.

5) Set the OSC OUT - REF FREQ INPUT switch to OSC OUT unless an external reference frequency is to be used.

2.7.1 Remote Connector

The control lines and their properties are described in Table 2-5, Remote Connector Pin Numbers. It is designed to be controlled by relay contact closure or by a logic zero from an RTL, DTL, or T^2L logic system.

Table 2-5. Remote Connector Pin Numbers

UNLESS OTHERWISE NOTED:

Logic LO: -0.5 V to +0.25 V. Input Load: 7 DTL gate circuits. (Typical current sink required is 12 mA.)

Logic HI: +3.5 V to +12 V.

Pin No.	Selected Mode	Characteristics
5 6 7 8 9 10 11 12 13	10 s 1 s 0.1 s 10 ms 1 ms 0.1 ms 10 μs 1 μs 0.1 μs TIME BASE	HI: No time base selected. LO: Any one input LO will select the respective time base. If more than one input is LO, the fastest time base will occur.
22 23 24 27 34 35 36	TEST FREQ BURST TIME A-B RATIO PERIOD AVG PERIOD FUNCTION	HI: No function selected. LO: Any one input low will select the respective function. More than one input LO will result in an indeterminate function.
25 26	COUNT HOLD	HI: Counter gate remains in previously selected state. LO: For greater than or equal to 500 ns will switch the gate to the selected state. Selecting both inputs will place the gate in the HOLD state.
31 32	START STOP SLOPE	HI: Negative slope. LO: Selected slope is positive.
33	B Enable	HI: A INPUT is connected to count chain. LO: A INPUT is not used and B INPUT is connected to count chain.
21	Fast Display	HI: Display time is controlled by front-panel controls of HOLD-VARIABLE-MIN and DISPLAY TIME. (Also, see remote display time, pins 17 and 18.) LO: Display time fixed at 40 μs nominal.
17 18	Display Time	Resistance: When the front-panel HOLD-VARIABLE-MIN switch is placed in the HOLD position, the display time can be controlled externally by placing a 500 KΩ variable resistor across pins 17 and 18. When 500 KΩ, display time is 10 seconds nominal. When 0Ω, display time is 100 ms nominal. If external resistor is applied, it will affect the control range of the front-panel controls reducing the 10 s maximum time when not in REMOTE mode.

continued . . . .

Table 2-5. Remote Connector Pin Numbers - continued

Pin No.	Selected Mode	Characteristics
20	RESET	HI: No effect. LO: For greater than or equal to 1 μs will reset the counter function and data storage. Counter will not be released to take a new count until returned to HI.
19	Ground	Logic Ground: May be used as reference point or source of LO signals, or program return point if program inhibit is not desired.
14	Ground, REMOTE Function	Output - HI: When front-panel FUNCTION switch is in any position other than REMOTE. LO: When in REMOTE position. Provides remote program inhibit when not in REMOTE mode. Load is a switch to ground for LO and 1KΩ to +5 V for HI.
15 16	A B Trigger Level	Analog: Input points for trigger level voltages. A ±15 V dc voltage will vary the trigger level greater than ±1 V x Attenuator setting on the front-panel control. The front-panel trigger level control must be in the preset position, otherwise excessive loading will result depending upon the front-panel trigger level pot position. Load resistance is 3 KΩ when in preset position.
3, 30 2, 29 1, 28	AC/DC x10 Atten. x100 Atten. C11 Option	HI: Selects AC. LO: Selects DC. NOTE: Pins 3, 2, 1: 'A' channel only. Pins 30, 29, 28: 'B' channel only.

2.8 USING A DIGITAL RECORDER

The Counter-Timer accommodates wide varieties of digital recorders, including the latest generation of high-speed line printers. An inhibit signal from the printer can be used to synchronize the counter recycle time with the print time.

2.8.1 Output Connector

Four-line 1-2-4-8 BCD data is provided at J10 on the rear panel. A binary '0' is 0 to +0.5 volt, a binary '1' is +5 volts with a 640 ohm nominal source resistance. The print command is a binary '1' with a 10 microsecond nominal duration.

NOTE

For synchronization, the inhibit signal from the printer must return in less than 10 microseconds with the DISPLAY TIME switch in the MIN position. With the DISPLAY TIME switch in the VARIABLE position, the measurement rate can be extended out to 10 seconds with the control knob.

Each decimal digit of the counter output is represented by four binary digits, or bits, which are weighted 1, 2, 4, and 8, respectively. To convert from binary to decimal, multiply the value of each bit by its weighting factor and add the products together. For example, binary 1001 is equivalent to 1 + 0 + 0 + 8 = 9 in decimal.

Refer to Table 2-6 for digital recorder pin numbers.

Table 2-6. Digital Recorder Connector Pin Numbers

Pin No.	Decimal Digit	Binary Weight	Pin No.	Decimal Digit	Binary Weight	
1	1	1	26	5	4	
2	1	2	27	5	8	
3	1	4	28	6	1	
4	1	8	29	6	2	
5	2	1	30	6	4	
6	2	2	31	6	8	
7	2	4	32	7	1	
8	2	8	33	7	2	
9	3	1	34	7	4	
10	3	2	35	7	8	
11	3	4	36	8	1	
12	3	8	37	8	2	
13	4	1	38	8	4	
14	4	2	39	8	8	
15	4	4	40	9	1	Ninth Digit Option
16	4	8	41	9	2	
17	5	1	42	9	4	
18	5	2	43	9	8	
19	Accessory Command		44			
20	Ground		45	Ext. Inhibit		
21			46	Overflow Data		
22			47			
23			48			
24			49			
25			50			

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SECTION 3
THEORY OF OPERATION

3.1 GENERAL

In general, counting instruments can be described by the block diagram of Figure 3-1. The operational modes of these instruments can be divided into two general classifications, frequency modes and timing modes. In the frequency modes, a precise reference signal controls the gate, and an unknown signal is accumulated. In the timing modes, an unknown signal controls the gate, and a precise reference signal is accumulated.

The Frequency mode is a typical frequency mode, and the Time A-B, Period, and Period Average modes are typical timing modes. The Test mode is similar to a frequency mode in that the precise reference signal controls the gate, but in the Test mode, the precise reference signal is also accumulated. The Ratio mode is similar to the timing modes in that the precise reference signal is accumulated. But in the Ratio mode, one unknown input signal opens the gate and another unknown input signal closes the gate.

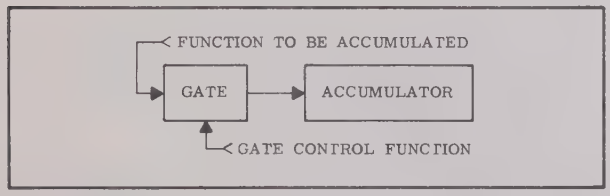

Figure 3-1. Simplified Block Diagram.

3.2 FUNCTIONAL DESCRIPTION

3.2.1 INPUT CIRCUITS

Input signals of varying amplitudes and shapes must be converted to digital form to enable the processing of the information with digital techniques. The functional blocks of the input circuits are shown in Figure 3-2.

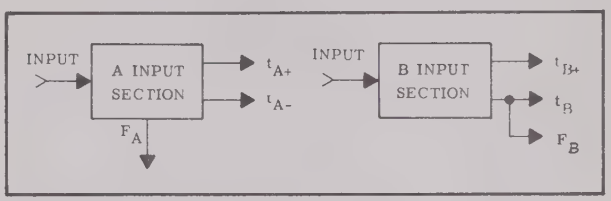

Figure 3-2. Functional Block Diagram.

Figure 3-3 shows a typical input signal applied to Channel A and the resulting waveforms generated by the Channel A input section. The t_{A+} and t_{A-} signals correspond to the times at which the input signal crosses the trigger level reference. The signal F_A, which is the same phase as t_{A+}, is a signal of digital form with the same frequency as the input signal.

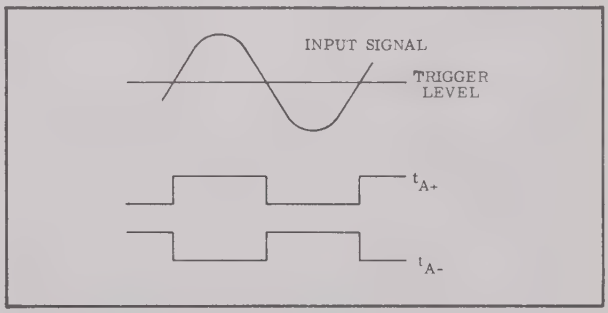

Figure 3-3. Typical Waveforms.

3.2.2 TIME BASE GENERATOR

The time base generator is composed of a precision reference oscillator and a series of decade counters. The general arrangement is shown in Figure 3-4.

Each of the decade counters divides the time base by a factor of ten. The number of divisions by ten may be selected on the front-panel switch or by remote program. The output of the time base generator controls the gate time in frequency modes, but is accumulated in timing modes.

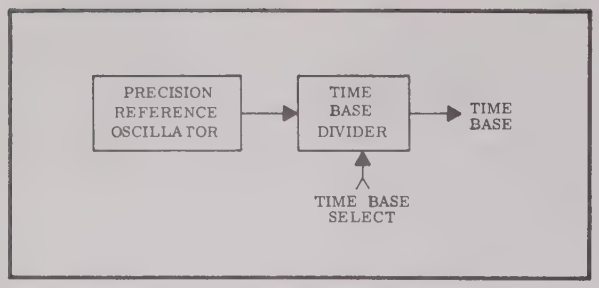

Figure 3-4. Time Base Generator.

3.2.3 ACCUMULATOR

When the gate is open, the signal to be accumulated is applied to a series of decade counters. These counters transform the serial decimal data into parallel binary coded decimal (BCD) data. This data is then temporarily stored in a memory. The memory is automatically updated each time the gate is opened and closed for a measurement. The stored BCD data is available for accessory equipment and it is also decoded for use in the display.

3.2.4 DISPLAY

The stored BCD data from the accumulator is decoded to parallel decimal data and applied to the display tubes. Legend and decimal point information are generated by the function logic for each mode and time base position.

3.2.5 FUNCTION LOGIC

The function logic is the nerve center of the counter. It accepts inputs from the front-panel switches or from a remote programming source and makes the decisions necessary to accomplish the selected functions.

The function logic is composed of two basic sections. One section generates dimensional information and the other section generates the logic controls to format the measurement selected.

The dimensional section generates the appropriate legend and decimal point data for each function and time base position. The other section is the master control of the counter. This section provides the proper time base division factor, selects the proper function to be accumulated, and selects the proper gate control function for each mode of operation.

3.2.6 RECYCLE CONTROL

The recycle control is a sequencer that produces various signals to control the measurement process. The recycle control generates reset, print and store commands and controls the minimum time between measurements.

3.3 DETAILED THEORY OF OPERATION

3.3.1 INPUT SECTION

3.3.1.1 Channel A

The basic input circuit is shown in block diagram form in Figure 3-5 and in simplified schematic form in Figure 3-6.

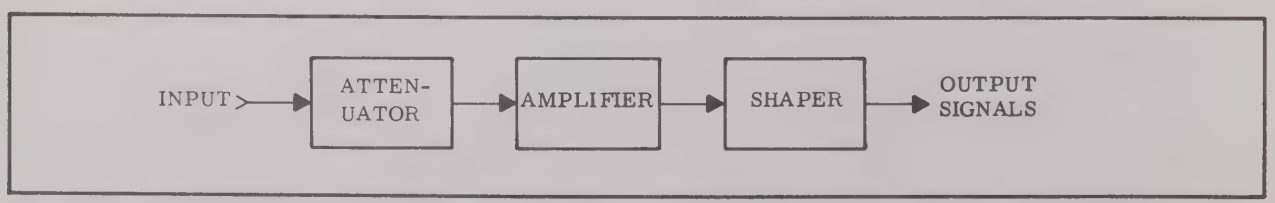

Figure 3-5. Input Circuit Block Diagram.

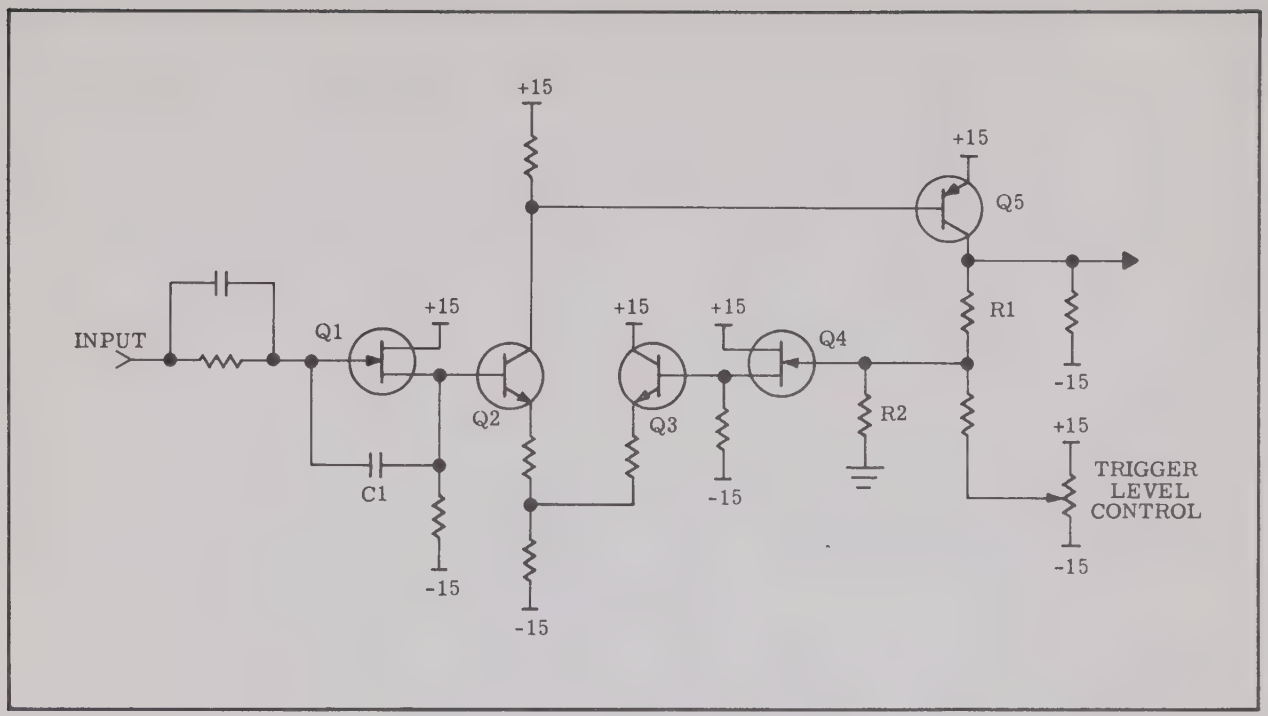

Figure 3-6. Simplified Input Circuit Schematic.

The attenuator is an RC network that provides attenuation factors of 1, 10 and 100. Field effect transistor (FET) Q1 is in a source follower configuration to provide a high input impedance.

Low frequency signals are coupled to Q2 through Q1, while high frequency signals are coupled to Q2 through C1. Q1 and Q2 form a wide-band differential amplifier with Q5 as the output stage. Q4 supplies negative dc feedback to provide the proper transfer function. The trigger level adjustment is connected to the gate of Q4.

The output of the amplifier (collector of Q5) is connected to the Schmitt trigger shown in simplified form in Figure 3-7.

The Zener diode CR1 and capacitor C1 provide a feedback path for emitter coupled transistors Q1 and Q2. Zener diode CR2, along with R1 and R2, fix the output voltage on Q2 collector at approximately 1 volt peak-to-peak on a 9 volt dc reference. The output of the Schmitt trigger is connected to the slope drivers shown in Figure 3-8.

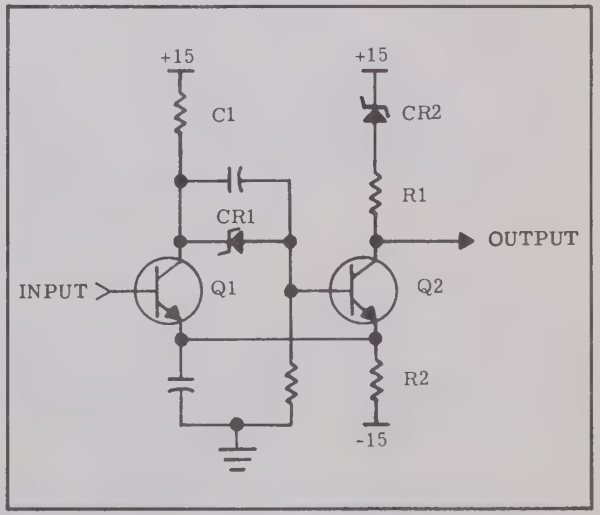

Figure 3-7. Schmitt Trigger, Simplified.

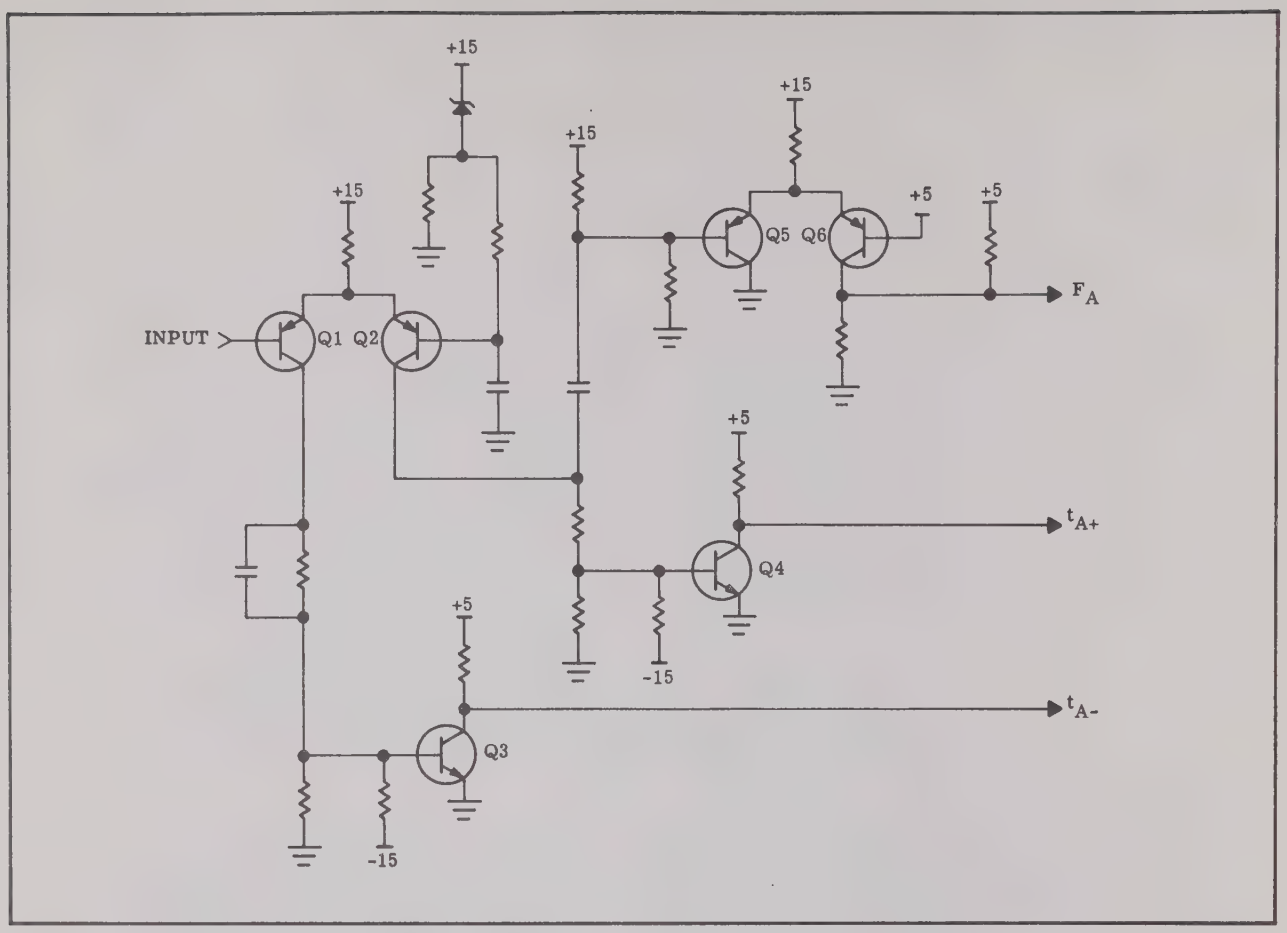

Figure 3-8. A Channel Slope Drivers.

The differential amplifier (Q1 and Q2) provides two signals of opposite phase. These are amplified by Q3 and Q4 for the positive and negative slope signals t_{A+} and t_{A-}. The differential amplifier composed of Q5 and Q6 produces the signal F_A, which is used for counting purposes.

3.3.1.2 Channel B

The B Channel is similar to the A Channel through the Schmitt trigger stage. The B Channel slope drivers are shown in Figure 3-9.

The opposite phase outputs of the Schmitt trigger are used to provide the inputs to the slope drivers. The timing signal t_{B-} is used to generate F_B for counting purposes. The schematic of Figure 3-10 shows how this is accomplished.

The timing signal is ac coupled to gate Z1. The diodes CR1 and CR2 protect Z1 from excessive input voltage transients.

3.3.1.3 Burst Detector

The A Input section contains a peak detecting circuit for use in the Burst mode. When the counter is in this mode, the peak detector senses incoming pulses and opens the gate. The circuit is shown in Figure 3-11.

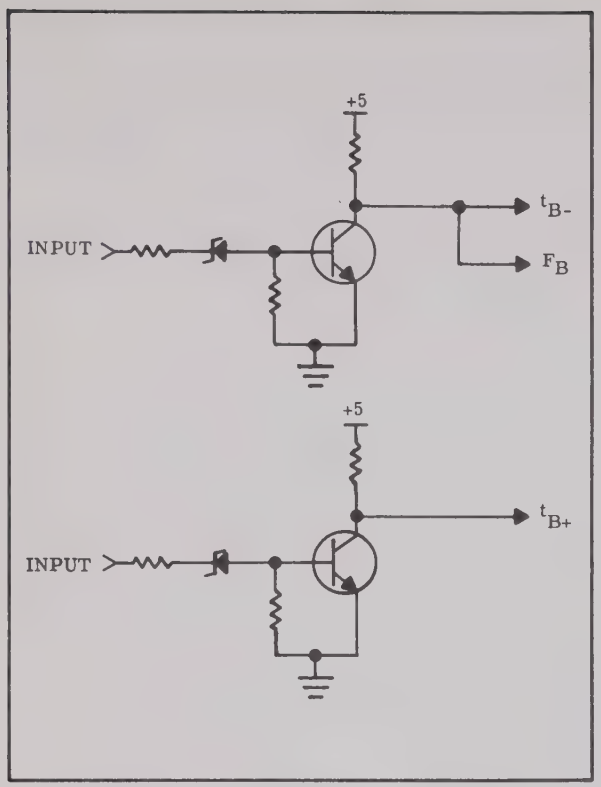

Figure 3-9. B Channel Slope Drivers.

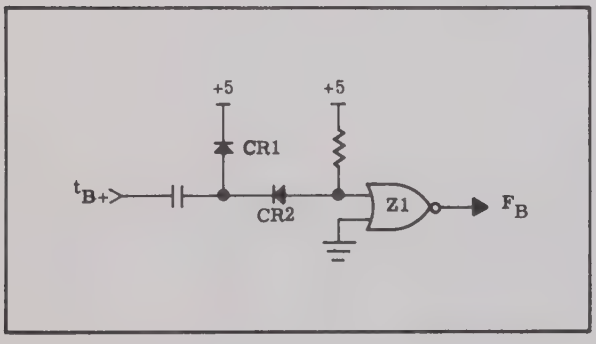

Figure 3-10. F_B Generator.

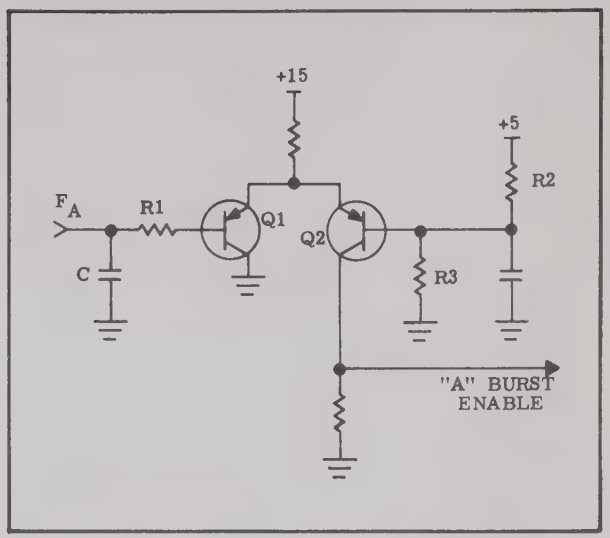

Figure 3-11. Burst Detector.

The signal F_A is filtered by the RC combination of C and R1. This signal is applied to the differential amplifier composed of Q1 and Q2. R2 and R3 provide a threshold of approximately 3.8 volts dc. When the integrated F_A signal approaches 3.8 volts dc, the "A" Burst Enable signal switches to approximately 3.2 volts dc. This voltage level is sufficient for a logic 1 state. For a discussion of how this signal opens the gate, see Section 3.3.5 (page 3-11).

3.3.2 TIME BASE GENERATOR

3.3.2.1 Oscillator and Multiplier

A block diagram of the time base divider section is shown in Figure 3-12.

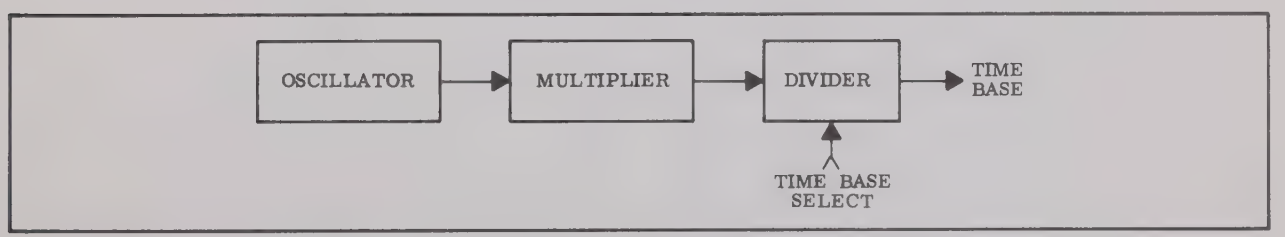

Figure 3-12. Time Base Divider Block Diagram.

A crystal-controlled Colpitts type oscillator, Figure 3-13, generates a 5 MHz sine wave. C1 provides frequency adjustment capability and R1 provides amplitude adjustment capability. The FET buffer, Q2, minimizes loading of the oscillator.

The switch either connects the internal oscillator to the multiplier section and switches the multiplier output to the output connector, or it applies an external reference signal to the input of the multiplier. (NOTE: For external reference specifications, see Table 1-1.) The emitter follower buffer, Q3, minimizes loading on the external reference generator, or isolates the internal oscillator from the multiplier.

A schematic of the multiplier is shown in Figure 3-14. The output of the buffer is ac coupled to a common emitter switch, Q1, that is either saturated or cut off, depending on the state of the buffer output. The collector of the switch is clamped through diode CR1 to +5 volts dc. (The collector resistor is connected to a supply voltage of +15 volts dc.) The clamp produces the linear output shown in Figure 3-15, when Q1 is turned off. C1 and R1 differentiate the output waveform, producing the current impulses shown in Figure 3-15.

Since Q2 is a common emitter NPN amplifier, the negative impulses have no effect on it. The positive impulses, however, cause an impulse of current in the collector circuit of Q2. This collector is connected to a high Q tank circuit resonant at 10 MHz. The input pulses cause the tank circuit to oscillate and produce the waveform shown in Figure 3-16. The Q of the tank circuit is such that approximately three percent of the signal energy is lost between input pulses.

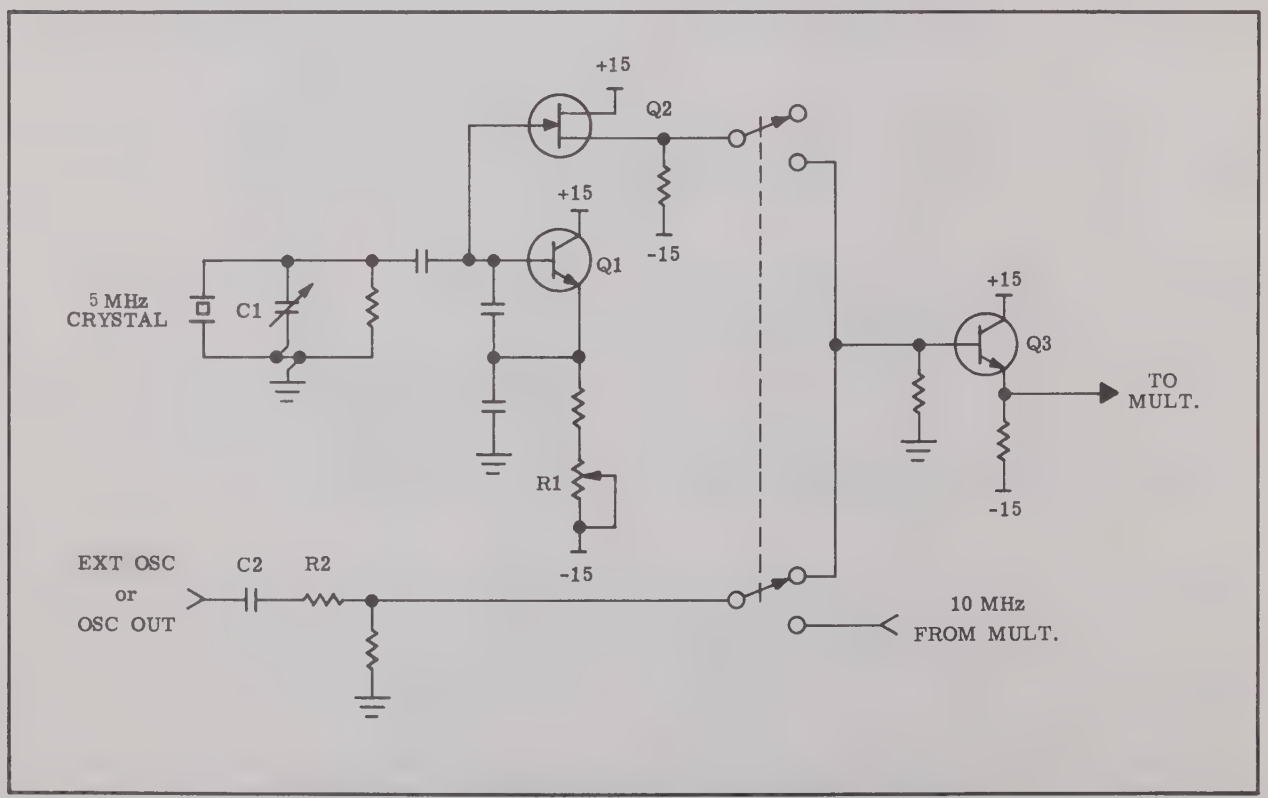

Figure 3-13. Crystal-Controlled Colpitts Type Oscillator.

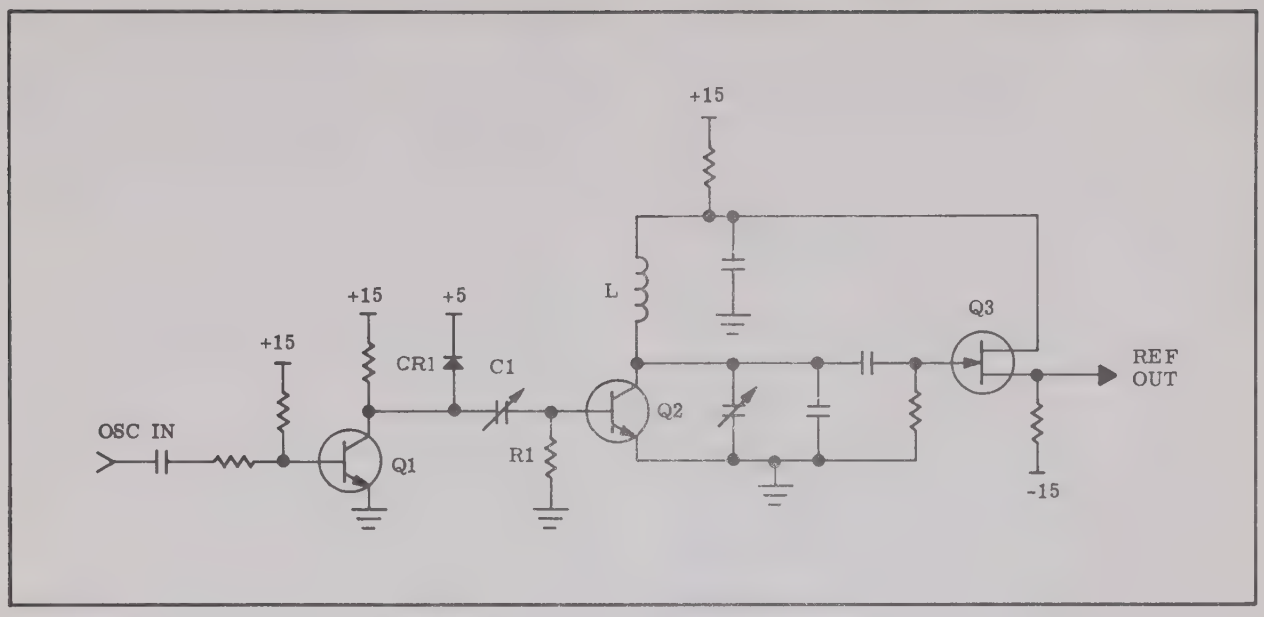

Figure 3-14. Multiplier Schematic.

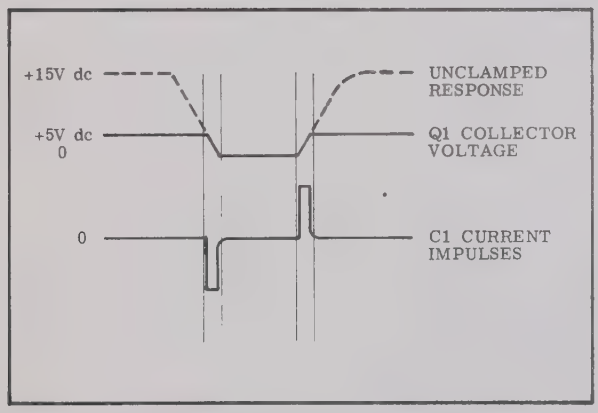

Figure 3-15. Differentiator Output Waveforms.

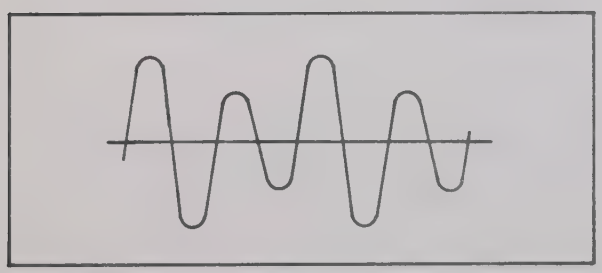

Figure 3-16. Tank Circuit Waveform.

A FET buffer, Q3, is used to provide a high impedance to the tank circuit to minimize loading effects. The multiplier output is buffered by a common emitter switch (not shown in Figure 3-14) for use in the counter. A similar buffer, with appropriate short circuit protection (also not shown in Figure 3-14), provides a time base output for use by accessory equipment.

3.3.2.2 Time Base Divider

The output of the multiplier is applied to the time base divider, which is composed of eight decade counters in a serial configuration. For a discussion of the operation of the decade counter, see the Troubleshooting section, paragraph 4.3.5.4. A set of typical waveforms is shown in Figure 3-17. Note that the R_9 function sets the counter to the digital number 9, or the binary coded decimal (BCD) number 1001. Also note that the D output frequency is one-tenth of the input frequency.

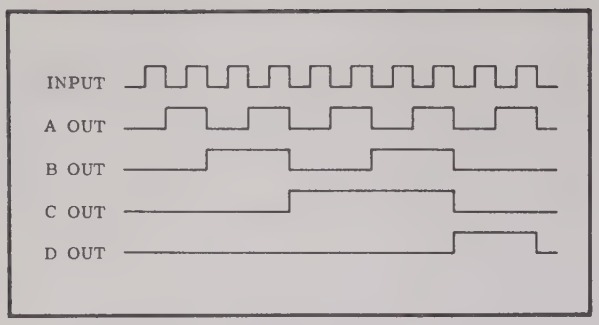

Figure 3-17. Typical Waveforms - Decade Counter.

The number of decade counters required to generate a given gate time is controlled by the front-panel TIME BASE selector switch through a series of gates. Figure 3-18 shows three decade counters connected in series for the purpose of this discussion. This instrument has eight decade counters each connected in a similar manner. For the theory and operation of the logic gates, refer to paragraph 4.4.2 (Section 4 of this manual).

Assume that the system has just received a reset command. The reset command is a false pulse for a few microseconds on the normally true reset line. The outputs of Z1, Z3, and Z5 switch true during the reset pulse. The decade counters, Z2, Z4, and Z6, are then set to the decimal number 9 (BCD 1001).

If the 0.1 μs position has been selected, one of the inputs to gate Z1 is false. The first decade counter, Z2, is held at the decimal number 9 (BCD 1001). The incoming time base signal is not counted by Z2. With no input pulses applied to Z4 and Z6, they will remain at the reset position, the decimal number 9.

Assume that the switch is moved to the 1 μs position. Z4 is held at the 9 position when the input to Z3 is false and the input time base signal is counted by Z2. If the switch is in the 10 μs position, the time base is divided by Z2 and Z4, while Z6 is held in the 9 state. As shown in

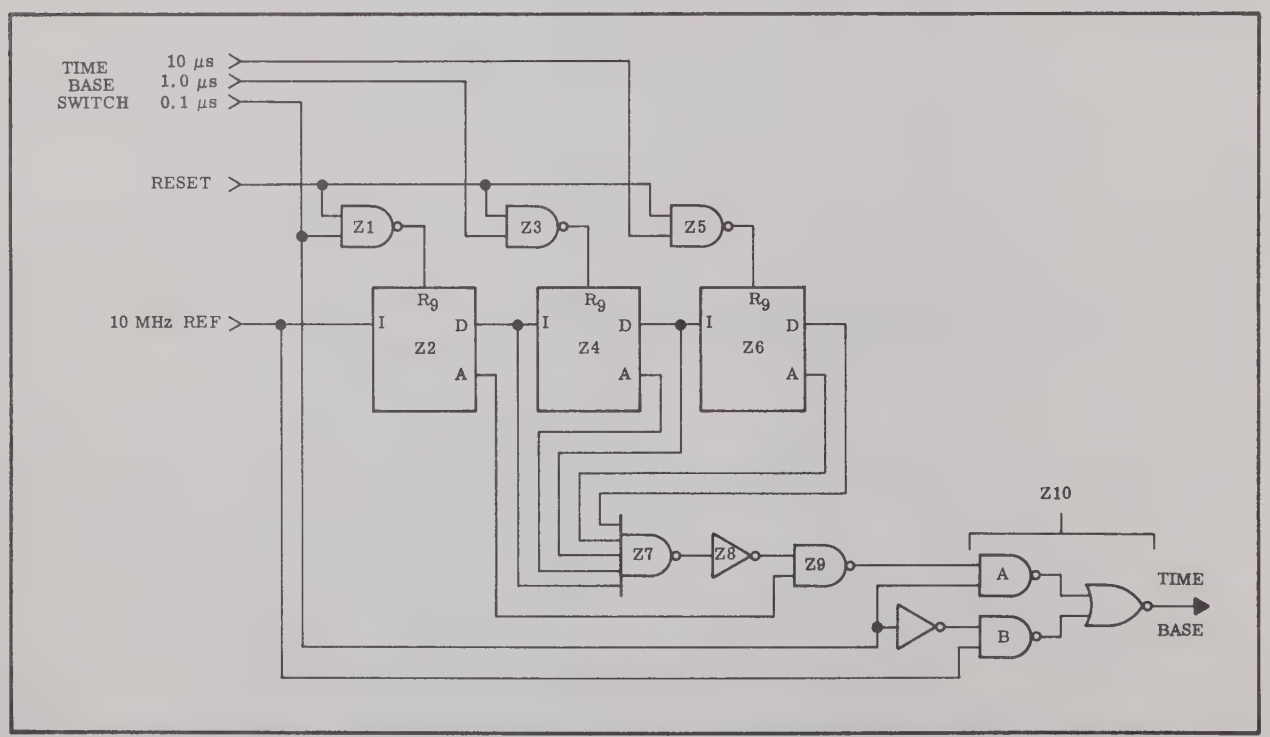

Figure 3-18. Serial Connection of Three Decade Counters.

Figure 3-18, the A and D outputs of the counters Z6 and Z9 are applied to the inputs of a NAND gate, Z7, with the A output of Z2. When the TIME BASE switch is in the 0.1 μs position, all of the counters are in the 9 state, which means their A and D outputs are true and the output of the NAND gate, Z7, is false.

Since the reset command sets all the counters to 9, the first pulse from the reference frequency causes all the counters before the one held to 9 to assume the decimal number 0 (BCD 0000). The output of Z7, therefore, becomes true on the first reference frequency pulse when the TIME BASE switch is in any position other than 0.1 μs.

When the switch is in the 1 μs position, the output of Z7 does not become false until Z2 has reached the count of 9. The time base has now been divided by 10. When the switch is in the 10 μs position, the output of the NAND gate, Z7, does not become false until Z2 and Z4 have both reached the 9 state, which means the time base has been divided by 100.

The output of Z9, the reference frequency output, and the 0.1 μs selection line are applied to the AND-OR-INVERT gate, Z10. If the 0.1 μs position has not been selected (the 0.1 μs line is high) Z10B is disabled and Z10A is enabled. The time base output is therefore the inverted output of Z9. If the 0.1 μs position has been selected, Z10A is disabled and Z10B is enabled. The time base output is therefore the reference frequency.

3.3.3 GATE CONTROL FUNCTION

The gate control function is generated by the circuit shown in Figure 3-19 (page 3-10).

The Count and Hold mode control signals are shown since they have direct access to the gate and override all other signals.

When the recycle control system generates a reset command, the reset line assumes a false state for approximately 20 microseconds. At all other times (except when another function generates a reset command) the reset line is true. The reset command causes the output of Z10 to assume a true state. Since Z9 and Z10 form the gate flip-flop, Z9 then assumes a false state. (See the diagram in Figure 4-9, page 4-16.) When the flip-flop is in this state, the gate is closed. (See the discussion on the gate, paragraph 4.3.6.8, page 4-11.)

If the Hold mode is selected, the input to Z2 is false, which causes the input to Z8 to be true. This in turn causes one of the inputs to Z10 to be false, which holds the output of Z10 true. Therefore, the gate is closed while the counter is in the Hold mode.

If the Count mode is selected, one of the inputs to Z9 is false, which causes Z10 to switch to a true state. Therefore, the gate is open when the counter is in the Count mode.

All control functions except Count and Hold have access to the gate through Z3 and Z4. Assume that neither the Count nor Hold modes have been selected and that the gate is closed. Assume further that all of the inputs to Z3 are true, causing its output to be false. If one of the inputs switches to a false state, causing the output to switch to true, the RC network differentiates the transition and a positive pulse appears at the input of Z7. The resultant negative transition at the input to Z9 causes the gate flip-flop to change states and open the gate. The false output of Z10 causes the output Z6 to become true. Since the reset line is true (in the absence of a reset command), the output of Z5 is false.

Therefore, any further start commands will not be accepted by Z3. The true output of Z9 is applied to Z4 enabling it for a stop signal. When one of the inputs to Z4 goes false, the RC network causes a positive transient at the input of Z8. The resultant negative pulse at Z10 causes the gate flip-flop to again change states, closing the gate. The true output of Z10 reverse biases diode CR1, causing one input of Z6 to appear true. At this time, the recycle control system generates a reset command which causes the lockout flip-flop to switch to a true state. The true output of the lockout flip-flop enables Z3 to accept a start command.

In the Frequency and Test modes, the time base generator controls the gate (see paragraph 3.1). Assume that the system has just received a reset and the gate is closed. Assume further that the counter is in either the Frequency or Test mode, which means that the time base generator is controlling the gate. When the time base is enabled, a false to true transition is applied to Z3 and Z4. Since the gate is closed, Z4 is disabled and Z3 is enabled. The transition, therefore, has no effect on Z4, but a true to false transient appears at the input of Z7. This transient opens the gate and allows the input signal to be accumulated.

When the time base dividers have completed their cycle, the input to Z3 and Z4 goes false for one clock pulse (one cycle of the 10 MHz time base). Since Z3 is now disabled and Z4 is enabled, the false to true transition has no effect on Z3. The true to false transition at the output of Z4, however, closes the gate.

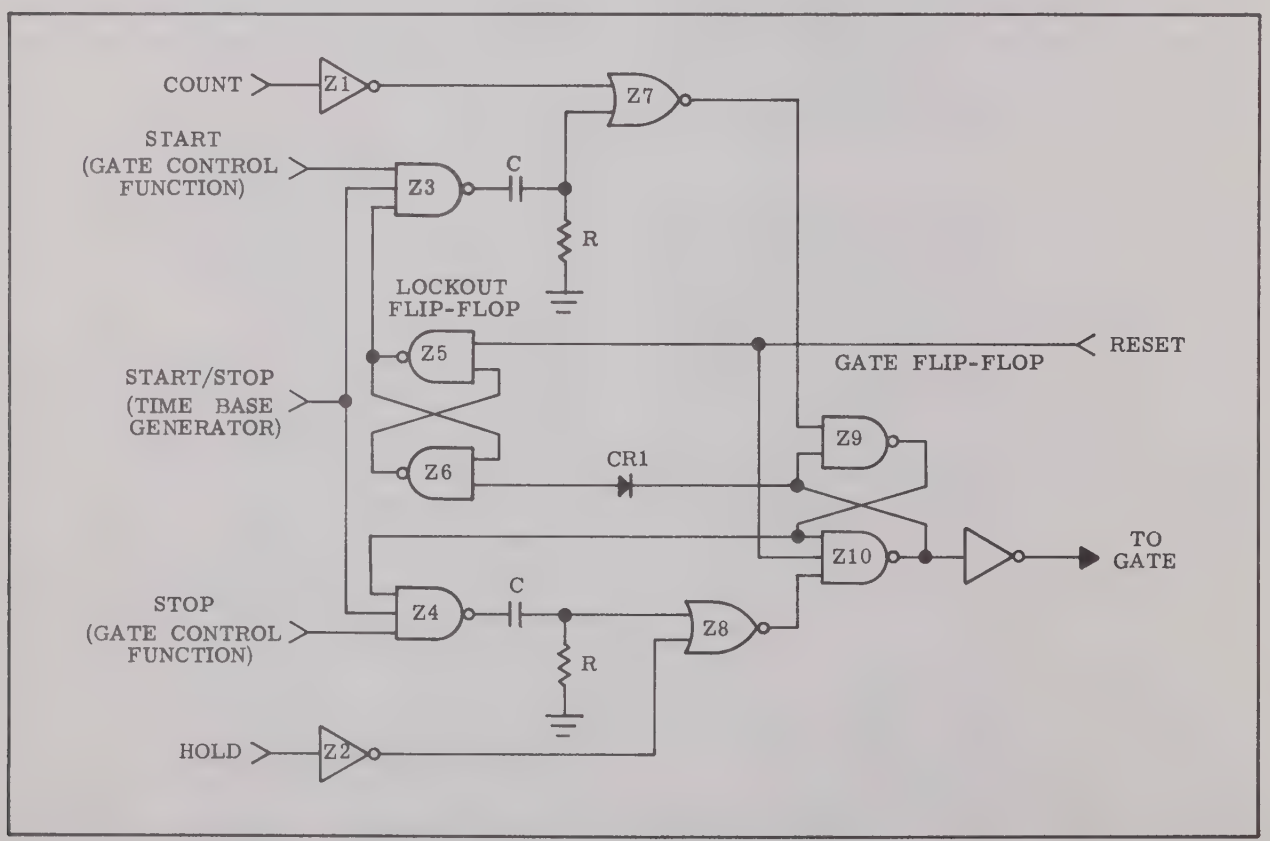

Figure 3-19. Gate Control Function.

3.3.4 GATE

The Gate and related circuitry is shown in Figure 3-20.

The Gate control function allows the enabled input to pass through to the accumulator when the gate control line is false. If Channel A is enabled, F_A is accumulated; if Channel B is enabled, F_B is accumulated; and if neither Channel A nor Channel B is enabled, the time base is accumulated. The function logic, paragraph 3.3.5, determines which input is accumulated.

3.3.5 FUNCTION LOGIC

A system of complex logic matrices generates input signals for the gate control function. The schematic of this system is shown in Figure 3-21. When a particular mode of operation is selected, the signal corresponding to that function in Figure 3-21 becomes false. It is easily seen, therefore, that when the Test, Frequency or Burst modes are selected, Z1 is enabled, allowing the 10 MHz time base to pass to Z2. Since neither the Ratio nor Period Average modes have been selected, Z3 is also enabled, allowing the 10 MHz time base to pass to the time base dividers. It can also be seen that the start slope, stop slope and B input signals determine which of the timing signals, t_{A+}, t_{A-}, t_{B+}, and t_{B-}, control the gate. In a similar manner, Figure 3-21 can be used in conjunction with the text of paragraph 3-1 to obtain a general understanding of each mode of operation. For a more detailed discussion, see the troubleshooting section.

3.3.6 BURST FLIP-FLOP

In the Burst mode, the time base is applied to the dividers and the gate is opened only when a burst of pulses is detected (see paragraph 3.3.5, Function Logic).

Either Channel A or B may be used in the Burst mode. The maximum frequency of Channel B is 10 MHz, while the maximum frequency of Channel A is 136 MHz. Because of the high-frequency input signals, the A Channel employs the peak detecting circuit described in paragraph 3.3.1.3 to generate an enabling signal. When Channel B is used in the Burst mode, the timing signal t_{B+} is used as the enabling signal.

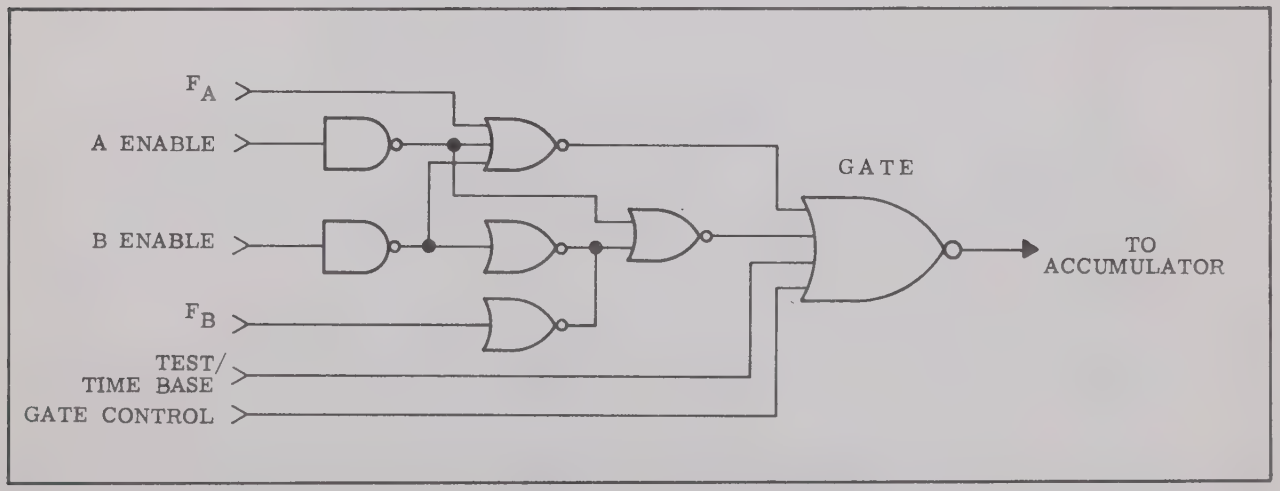

Figure 3-20. Gate.

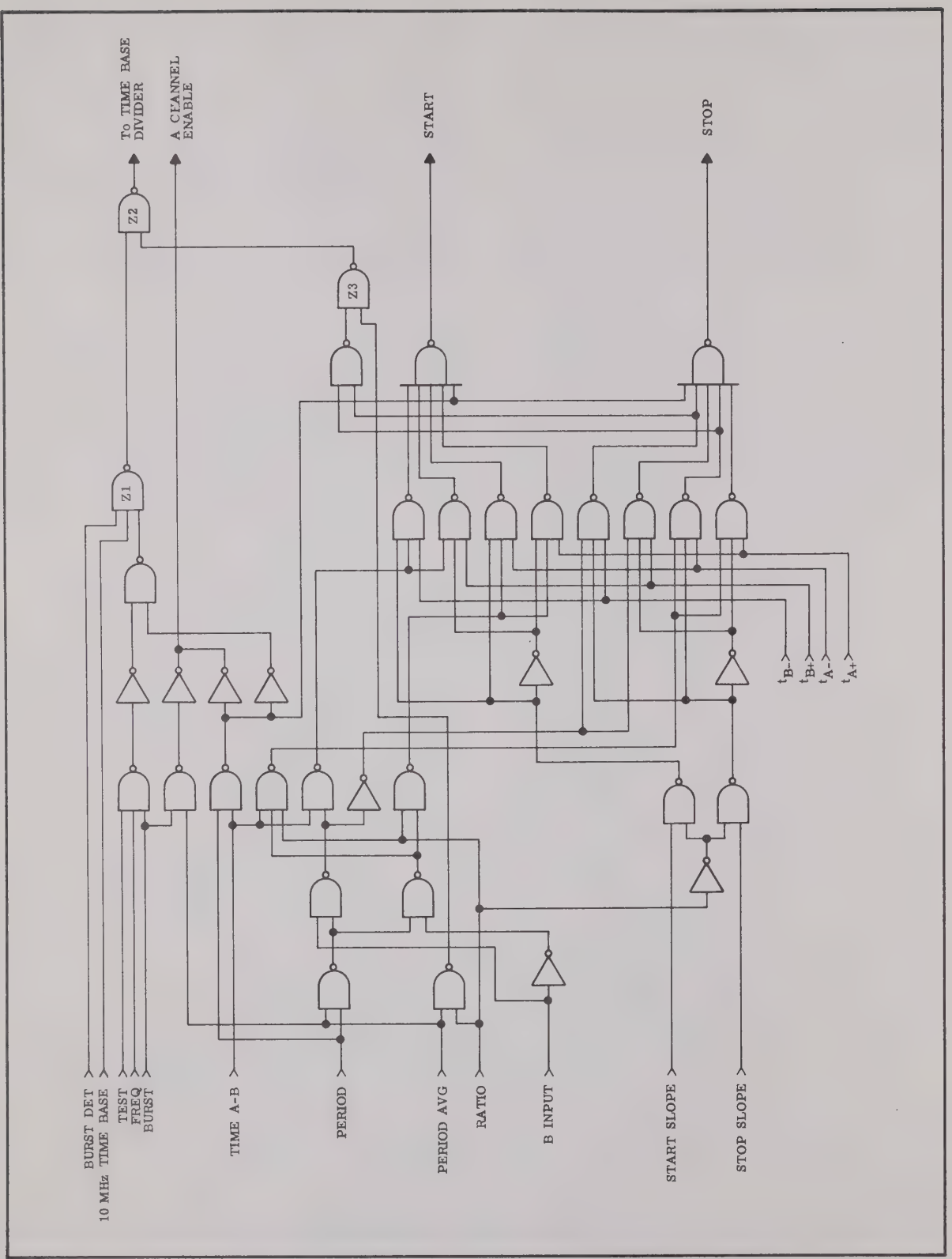

Figure 3-21. Function Logic.

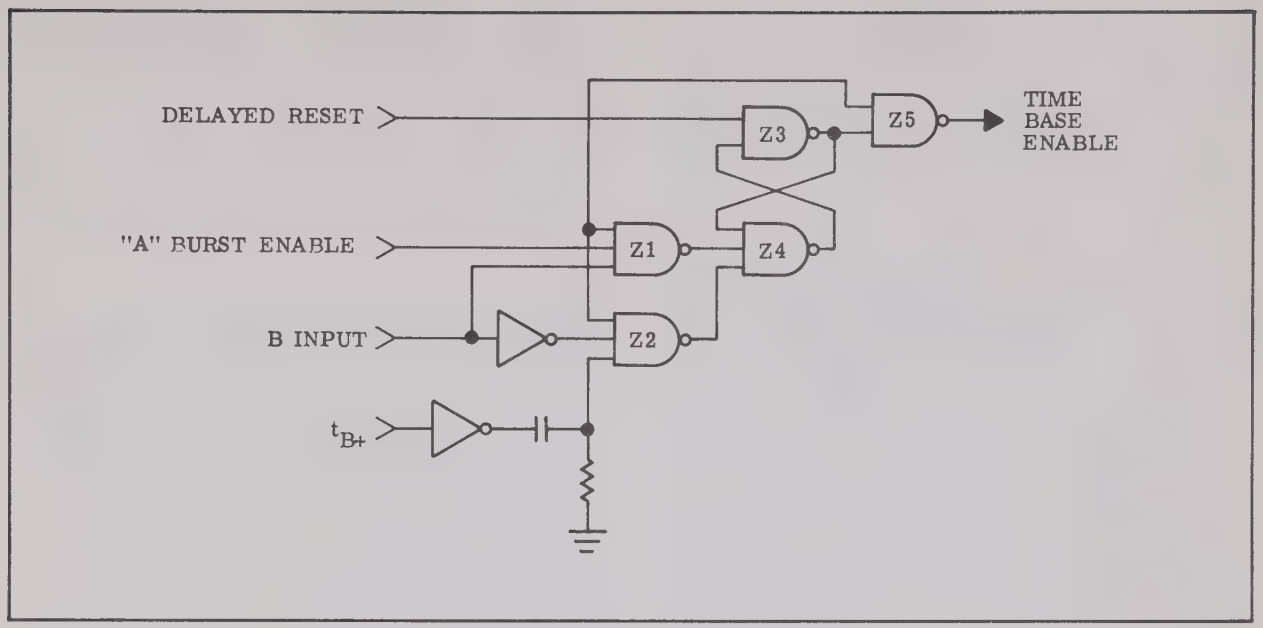

Figure 3-22. Burst Flip-Flop.

The circuit of Figure 3-22 generates the gate opening command from the enabling signals.

The output of Z3 is normally true, but when a "burst" is detected, it switches to a false state. The resulting true output of Z5 is applied to Z2 of Figure 3-22, the output of which opens the gate.

When the gate is closed, the store one-shot generates a pulse of approximately 5 microseconds in duration. The Type D flip-flops in the memory section update the information supplied to the display decoders during this time.

3.3.7 RECYCLE CONTROL

The recycle control system is a series of delay circuits (see Figures 4-4 and 4-5). The basic circuit used to obtain the various delays necessary is shown in Figure 3-23. This circuit is a simple one-shot.

The output is normally true, but switches false when a true to false transition appears at the input. The diode clamp protects the inverter from negative input levels. The period of the false output is determined by the RC network.

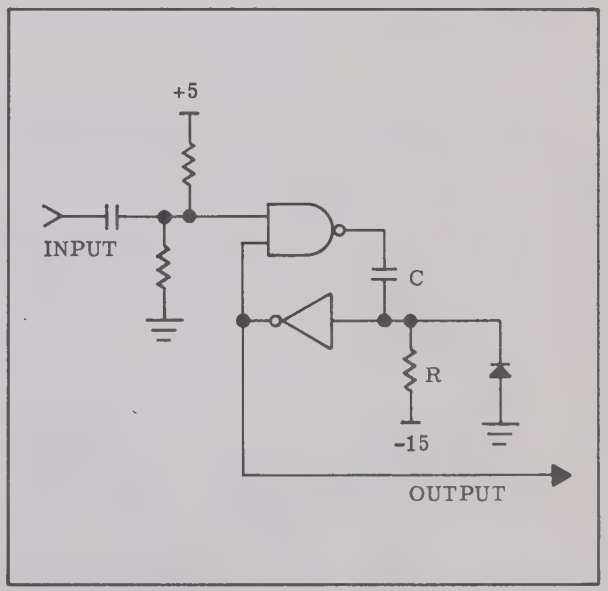

Figure 3-23. Typical One-Shot Circuit.

At the completion of the store pulse, the accessory command one-shot generates a pulse of approximately 10 microseconds in duration. This pulse and the updated information supplied to the display decoders are made available for use by a digital recorder.

At the completion of the accessory command, the display time generator produces a pulse that determines the length of time the new data is displayed. In the minimum display time mode, the display time generator is disabled. In the variable display time mode, the pulse width varies from 100 milliseconds to 10 seconds, depending on the position of the display time control. The display time generator circuit is shown in Figure 3-24.

In the variable display time mode, the display time flip-flop output, which is normally false, switches true on the negative slope of the accessory command. This causes the collector of Q2 to rise toward 5 volts dc. Capacitor C begins to charge through the display time control potentiometer, R1, and other series resistors. When the voltage at C reaches a predetermined threshold, both Q1 and Q2 saturate. R2 is very small in comparison to R1 and R3; therefore, C discharges rapidly. When Q2 saturates, the display time flip-flop is reset to its normally false state.

At the completion of the display time pulse, the reset one-shot generates a pulse of approximately 20 microseconds in length. This pulse is used to reset the gate, the time base dividers, the accumulator section, and the memory section. The circuit shown in Figure 3-25 is used to create a delayed reset signal. This circuit increases the reset pulse width to approximately 24 microseconds. The delayed reset signal disables the gate opening function until the gate has achieved stability.

For timing diagrams and a more detailed discussion of the actual circuit operation, see the troubleshooting section.

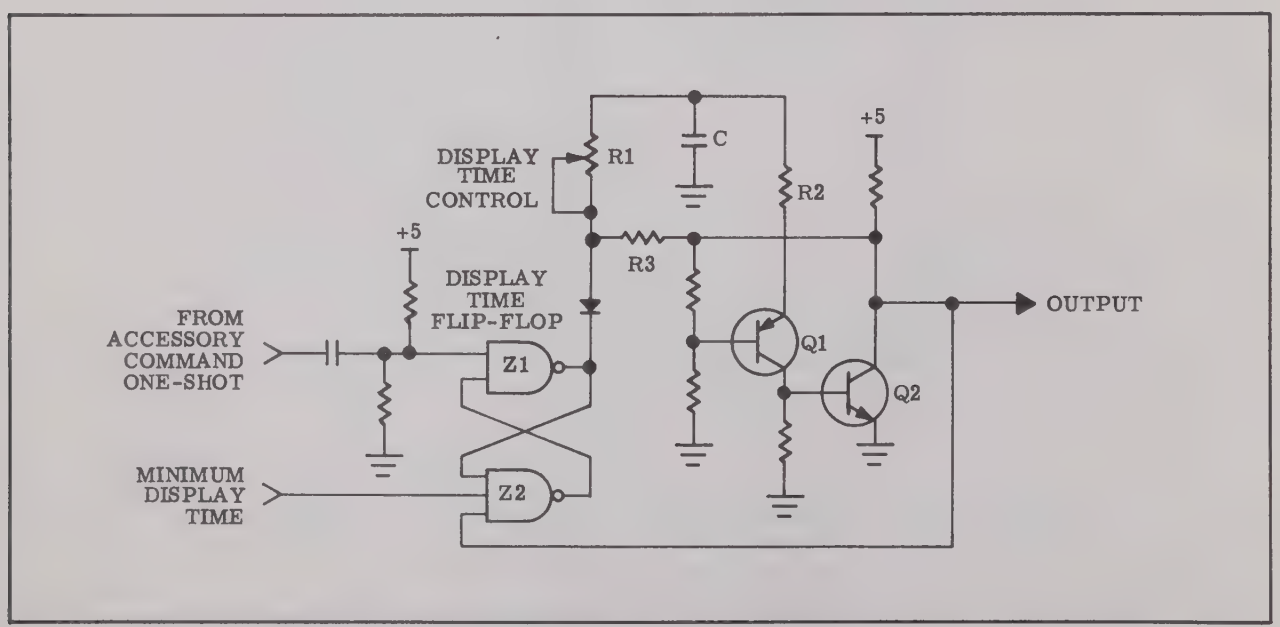

Figure 3-24. Display Time Generator.

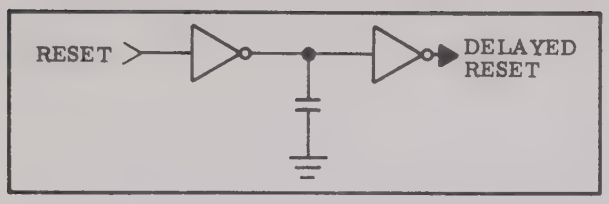

Figure 3-25. Delayed Reset Generator.

3.3.8 POWER SUPPLY

3.3.8.1 General

The power supply consists of four sections: line filter, power transformer, unregulated supplies and regulating amplifiers with their pass elements.

The instrument is isolated from the power line by a line filter which rejects line noise frequencies above 1 kHz. The filter also inhibits frequencies above 1 kHz that may be generated in the instrument, from being transmitted out the power line.

A 115/230 volt switch connects the two power transformer primaries in parallel for 115 volts, or in series for 230 volt operation. The secondaries provide the proper ac voltage for producing the unregulated dc supplies. The +15 volt and -15 volt unregulated supplies are derived from a common secondary winding.

Each unregulated supply uses a rectification system consisting of full-wave rectifiers and a large filter capacitor. Each system supplies a pulsating dc voltage which is smoothed by a filter capacitor to provide an unregulated dc voltage with nominal ripple voltage.

3.3.8.2 Overload Regulation

Each of the four unregulated supplies is regulated by means of a stable voltage reference, high-gain amplifier and a series pass element (see Figure 3-26). The unregulated dc voltage is connected to the series pass transistor which is a high impedance current source. When the instrument is energized, startup current is supplied to the high-gain amplifier from the unregulated dc supply by the startup resistor R_{ST} (see Figure 3-27). The amplifier turns on the series pass transistor which supplies current to charge the output loads. This action continues until the output rises to a greater voltage than V_R. At this time, an error signal is generated at the input of the amplifier as a result of the difference in potential between V_R and V_S, the sense voltage. The action of the error signal overrides the action of R_{ST}. The sense voltage is obtained from the junction of a voltage divider, R_A and R_B, which sense the output voltage.

The amplified error signal will cause the series pass transistor to supply enough current to the load to bring the output voltage to a level such that $V_R = V_S$. The output voltage at this time may be calculated from the formula

$$E_o = V_R \left(\frac{R_A}{R_B} + 1 \right)$$

The potentiometer, R_V, is provided to allow adjustment of the output voltage of the supplies to a precise level. Refer to Figure 3-27. An increase in the output load will cause the output voltage and the sense voltage to fall. The reference voltage remains constant. The resulting error signal is amplified by Q_B and Q_C and applied to the series pass transistor through the limiting resistor R_L. The amplified error signal increases the amount of current supplied by the series pass transistor to the output load, therefore increasing the output voltage to its original level.

The output of the power supply appears as a low source resistance to the load as a result of the negative feedback to the series pass transistor supplied by the high-gain amplifier.

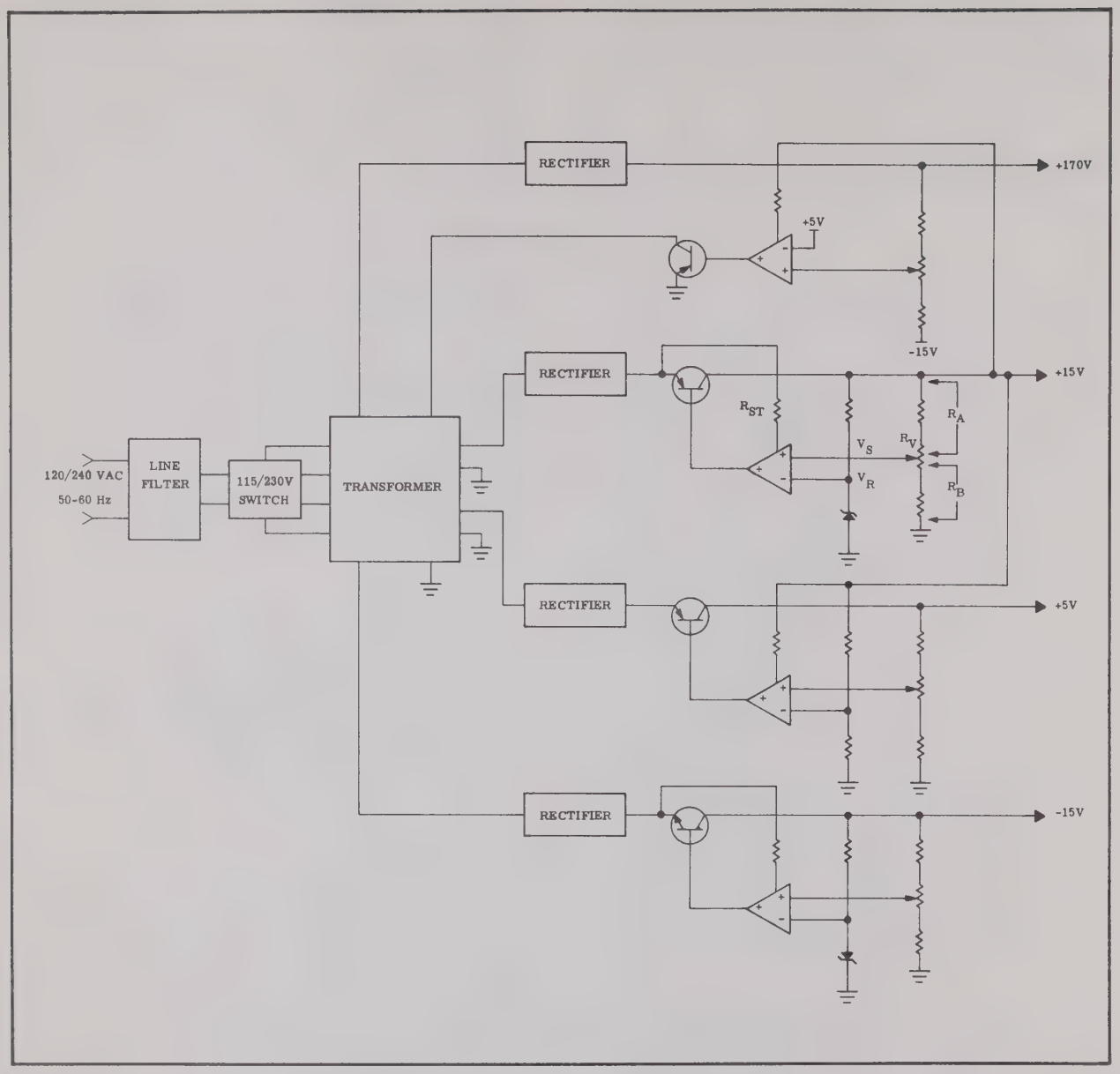

Figure 3-26. Power Supply Block Diagram.

3.3.8.3 Pass Elements

The series pass element acts as a high impedance to the ripple voltage on the unregulated dc supply. This gives a high first order rejection of the ripple voltage. Amplification and negative feedback further reduce the ripple component resulting in a stable dc output voltage with a low ripple function.

3.3.8.4 High Voltage Supply

The +170 volt supply differs as noted: The reference voltage is obtained from the +5 volt regulated supply. The output voltage divider is connected from the +170 volt regulated supply to the -15 volt regulated supply. The operation of the +170 volt supply can be likened to the operation of the other regulated supplies if their

output terminal is grounded and the ground terminal used as the output to the load.

The series pass transistor is connected between ground and the center tap of the high-voltage secondary of the power transformer.

The effective resistance of the series pass transistor is then varied to maintain a voltage drop across the series combination of the series pass transistor and a resistor that equals the difference between the unregulated dc voltage and +170 volts dc.

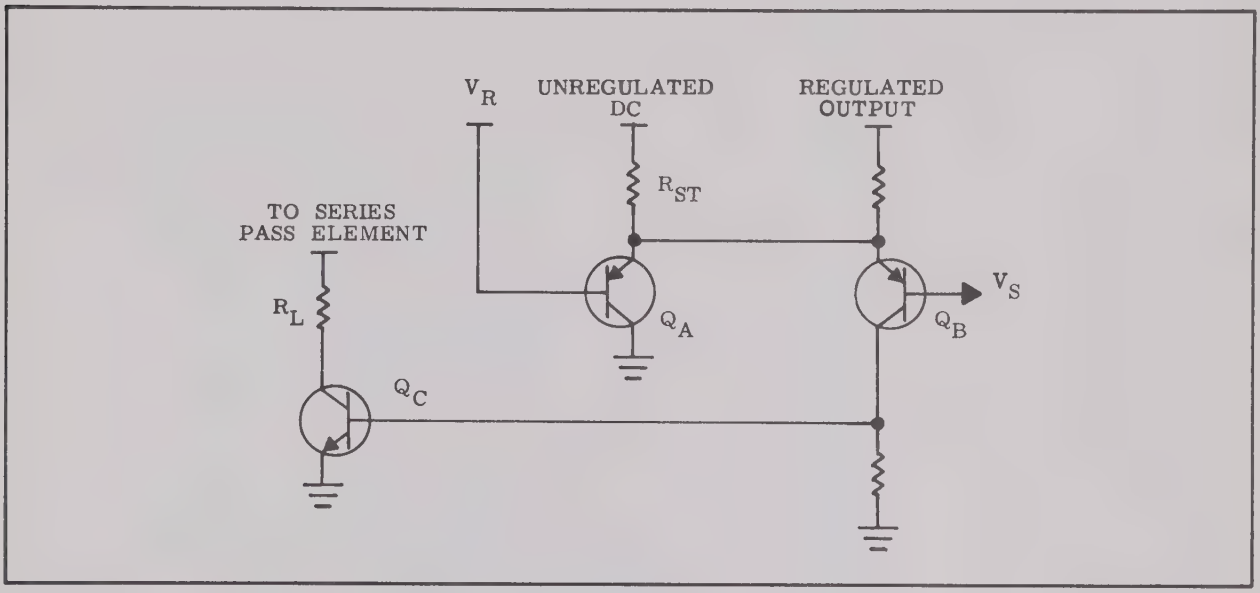

Figure 3-27. High-Gain Amplifier.

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SECTION 4
MAINTENANCE

4.1 GENERAL

This section describes maintenance procedures to sustain operation of the Counting Unit. The information includes preventive maintenance, adjustments, and troubleshooting. Preventive maintenance encompasses the periodic cleaning and visual inspection necessary to detect physical defects. Occasionally adjustments are required for the power supply and oscillator. Troubleshooting involves basic troubleshooting procedures that enable the technician to correct equipment malfunctions.

4.2 PREVENTIVE MAINTENANCE

Preventive maintenance is work performed on the equipment, usually when the equipment is not in use, to keep it in good working order so breakdowns and needless interruptions will be kept to a minimum.

4.2.1 CLEANING

Proper cleaning of the equipment will aid in minimizing breakdowns or malfunctions. The following cleaning methods may be used as applicable.

a) A clean, dry, lint-free cloth; a dry brush; or a vacuum cleaner may be used to remove loose dust, dirt, and lint.

b) If available, dry compressed air at a line pressure not exceeding 30 psi may be used to remove dust from inaccessible places, provided that care is exercised to prevent transfer of dirt to nearby parts. Care must also be exercised to ensure that damage to components does not result from the air blast.

c) Corrosion should be removed with fine crocus cloth (No. 000). Emery paper or steel wool must never be used to clean near electrical equipment; the particles that come from such material are conductive and can create short circuits. All dust and metallic particles should be removed by compressed air or vacuum cleaning. If compressed air is used, prevent the scattering of particles to magnetic parts.

d) After corrosion is removed, the affected surface should be treated with paint and/or moisture-and-fungus resistant Krylon.

e) Pure ethyl alcohol may be used to clean connector contacts and to remove excess rosin flux; it must not be used, however, to clean insulating varnish.

4.2.2 VISUAL INSPECTION

After cleaning the equipment, inspect carefully before restoring it to operation. The inspection should include the following:

a) Check the fuse, either visually or with an ohmmeter.

b) Ensure that the oscillator and glow tubes are securely in place.

c) Check all components for damaged leads and loose connections.

d) Check to see that switches have not been inadvertently placed at the wrong settings.

e) Check for smooth rotation of the DISPLAY TIME control from extreme counterclockwise to extreme clockwise.

f) Examine the printed circuit board and the components for signs of overheating.

g) Ensure that there is adequate air circulation for the equipment.

> **CAUTION**
>
> BEFORE ATTEMPTING TO ISOLATE AN INSTRUMENT MALFUNCTION, REMOVE ALL SYSTEM INTERFACE CONNECTIONS; i.e., REMOTE INPUT, DIGITAL RECORDER, etc.

4.3 TROUBLESHOOTING

This is a complex electronic instrument, and there is no simple way of locating troubles. A thorough understanding of the functions of the logic circuits is the best help (see Section 3, Theory of Operation). The signal flow is shown in the block diagram (Figure 4-1); timing and control signals are illustrated in Figure 4-5.

With an understanding of the circuits, a technician should be able to make a reasonable assumption as to the general source of trouble based on the symptoms.

Frequently, a visual inspection and a systematic approach to the troubleshooting problem may be more rewarding than a haphazard check of voltages and waveforms. The following instructions are presented as an aid in formulating the systematic approach.

4.3.1 BASIC TROUBLESHOOTING PROCEDURES

In troubleshooting electronic equipment, sources of problems can be divided into two categories: improper operating procedures and equipment malfunctions. The first category, since it deals with human error, is a more prevalent source of equipment problems than most people care to admit. Therefore, this category should always be investigated and eliminated before it is assumed that a valid equipment malfunction exists. After eliminating all possibility of human error, an equipment malfunction can, with assurance, be systematically attacked. It is vitally important to define the problem before attempting to solve it. The basic procedure consists of the following steps:

(1) Examine the evidence of trouble.

(2) Look for obvious solutions first.

(3) Isolate the problem to a major functional area.

(4) Analyze the reduced problem area for final solution.

(5) Correct the difficulty.

(6) Restore conditions for normal operation.

(1) Examine Evidence of Trouble

Take time to study the problem thoroughly. For example, if the display indicates erroneous information, note whether the trouble is general or whether the error applies to one or two decades only. Examine the data reaching the display; it should be in agreement with the data on the storage register. Gather clues from all accessible check points:

a) TEST mode operation; TRIGGER lights; GATE indicator.

b) The visual display.

c) Circuit board test points.

d) Printed records from external sources (when available).

In evaluating indications from the various checkpoints, determine particularly whether a disagreement exists between various related functions.

(2) Look for Obvious Solutions First

Question the coincidence of failure with other recent events, such as cleaning or servicing. Human errors sometimes result in accidentally displaced control settings. Quite often the solution to a difficulty will become self-evident through thoughtful analysis of immediate indications.

(3) Isolate Problem to a Major Functional Area

Although the equipment is an integrated network of functional activities, for troubleshooting purposes it is convenient to subdivide it into its major functional circuits. (See the Block Diagram on Page 5-1 for location.) To locate various components, see the individual assembly drawings in Section 5. The block diagrams in this section show the individual functional sections.

As the troubleshooter develops a working knowledge of the overall equipment, he will experience little difficulty with this isolation step. Isolating the disorder to an individual functional circuit can be accomplished either by a method of direct association or through a process of elimination.

(4) Analyze Reduced Problem Area for Final Solution

Once the investigation has been narrowed down to a restricted circuit area, the rest of the unit can be temporarily ignored.

(5) Correct the Difficulty

When the final solution has been reached, and the defective or faulty part has been pinpointed, remedy the fault by replacing the component as required. Some remedies, however, may call for performing a repair on one of the relatively few assemblies that is not designed for instant removal and replacement. Typical of these items is a break in the circuit board etching.

(6) Restore Conditions for Normal Operation

When all remedies have been completed, make sure that the unit is returned to normal operating condition. If controls have been changed to facilitate troubleshooting, reset them. Note particularly that all circuit board components are in and secured, and all switches are set properly.

4.3.2 REPAIR

Once a trouble is traced to a defective individual part, replacement should be made with identical parts, if practical. Refer to the drawings in Section 5 for correct values, tolerances, etc. When substitutions are necessary, use components that duplicate the originals in every possible respect. Avoid applying excessive heat to the printed circuit board by using a small iron and working quickly.

4.3.3 COVER REMOVAL

Simply loosen the two thumb screws in the two rear trim pieces. For top cover removal, slide the trim piece down and slide the cover to the rear and remove. To remove the bottom cover, slide the trim piece up and slide the cover to the rear.

4.3.4 TROUBLESHOOTING THE INPUT SECTION

> NOTE
>
> Refer to the block diagram in Figure 4-1 when troubleshooting the Input board.

4.3.4.1 Introduction

Troubleshooting should begin by observing front-panel indicators in various operating modes. The readout display and the GATE and TRIGGER level lamps will provide clues to malfunctions. Start and Stop pulses can be monitored at the rear panel.

4.3.4.2 Visual Indicators - GATE Lamp

The GATE lamp provides information about the counting gate. If the count gate is opening and closing correctly, the GATE lamp should flash on and off. If the gate light operation appears normal, and if no readout is apparent, we will consider the trouble to be in the Input section.

4.3.4.3 Removal of Function Board

To gain access to the Input board for troubleshooting, the Function board must first be removed. To remove the Function board, remove the four hold-down screws around the perimeter of the board, then remove the two No. 4 screws holding the 36-pin connector to the rear panel. Carefully slide the Function board forward and upward. The Function board should hinge on the wire harness which runs along the left-hand side of the board. Place a suitable insulative material, e.g., piece of cardboard, on top of the Regulator board and pivot the Function board over to the left and allow it to rest on this insulated material.

4.3.4.4 Test Function

Place the FUNCTION selector switch in TEST. Place the TIME BASE switch in any convenient time base between 1 μs and 10 s. The display should read 10 MHz in any of these time base positions.

> NOTE
>
> In the TEST function, the input amplifiers are not tested. The internal reference is routed to the first decade and counted.

4.3.4.5 Detailed Troubleshooting of the Attenuators

To test the attenuators, connect a BNC cable from the OSC OUT - REF FREQ IN jack at the rear panel to the input jack of the attenuator to be tested. With a scope, observe wire tie point M of the Input board if Channel A is to be tested, or wire tie point R of the Input board if Channel B is to be tested. The signal should appear at 1 volt rms in the X1 position. Attenuation by 10 would give 100 millivolts rms, and the X100 position should give 10 millivolts rms at point M or R. The operation of the attenuators are straightforward and a quick reference to the schematic diagram (dwg. no. D437036) should be all that is required to locate any trouble in the attenuators.

4.3.4.6 Detailed Troubleshooting of the A Channel Input Amplifier

Impedance matching between the attenuator and amplifier is performed by a field effect transistor (FET) in a source follower circuit configuration. The signal is coupled by the FET at low frequency and by C1 at higher frequencies to a wide-band differential amplifier comprised of Q2, Q3 and Q5. This amplifier employs negative feedback through source follower Q4 to achieve a flat gain curve. The trigger control

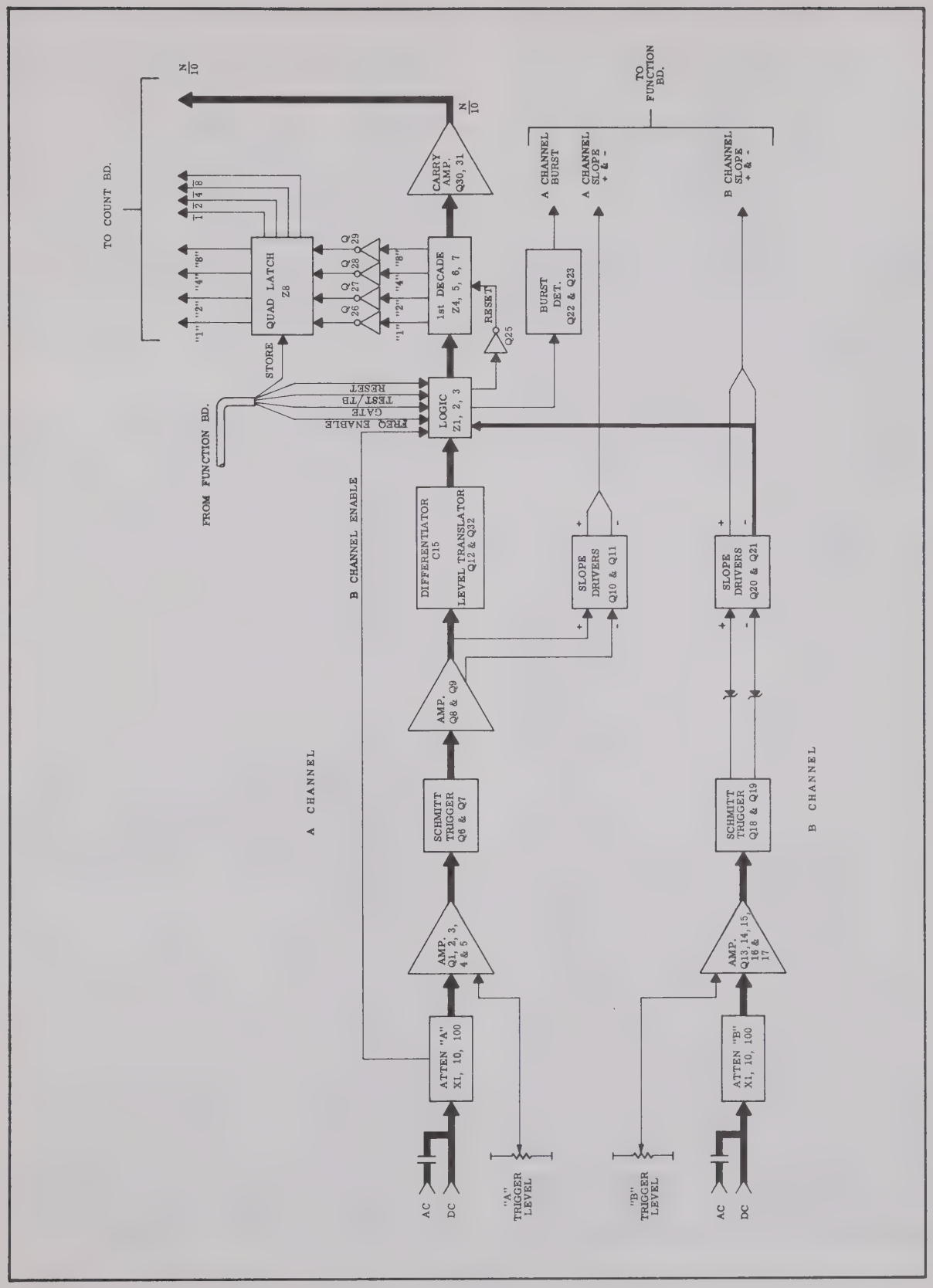


Figure 4-1. Input Board Block Diagram.

pot on the front panel is connected to the amplifier at the gate of Q4. The output of the amplifier, collector of Q5, drives Q6 and Q7 which are connected as a Schmitt trigger. The Schmitt trigger shapes the output of the amplifier to give a 1 volt peak-to-peak square wave applied to the base of Q8. Q8 and Q9 are connected differentially and together drive the slope output drivers, Q10 and Q11. The output of Q10 and Q11 appears at the Function board as an A Channel positive and negative slope signal. Translation of logic levels to operate the MECL logic is accomplished by Q12 and Q32. The output of Q9 is differentiated by C15 and amplified by differential pair, Q12 and Q32, which drive the MECL gate Z2. The output of Q32 is a pulse from approximately 3 to 5 volts and 3 to 5 nanoseconds in width.

4.3.4.7 Detailed Troubleshooting of the B Channel Input Amplifier

The B Channel Amplifier is similar in operation to the A Channel Amplifier described in the paragraph above, the differences being that the output of the Schmitt trigger drives the slope drivers directly through Zener diodes used as level translators. The outputs of Q20 and Q21 are routed to the Function board as B Channel positive and negative slope signals.

4.3.4.8 Detailed Troubleshooting of the Logic Selector Section

The outputs of the A and B Channels are applied to the logic selector section of the Input board. The output of Channel A is applied to Pin 5 of Z2 while the output of Channel B is applied to Pin 13 of Z3. The B Channel Enable, Pin 13 of Z1, selects the channel whose frequency will be counted. When the A Channel attenuator switch is placed in the B INPUT position, the output of Z1 Pin 11 goes to the logic 1 state, thus disabling Z2 allowing the output from Z3 Pin 11 to be accumulated. The test/time base information from Z3 Pin 2 contains the reference frequency output from the Function board. In the test/time base mode, this signal will be 10 MHz and will be passed by Z3 Pin 3 to Pin 11 of Z2 and will be counted if the instrument is gating. In frequency A, Z2 will have the frequency passed by A Channel applied to Pin 9.

In B Channel Enable, the output frequency of the B Channel will appear at Z2 Pin 10. The gate signal is applied to Z2 Pin 12. If Z2 Pin 12 is lower than 3 volts dc, the information applied to its inputs will pass to Pin 8, its output, and be accumulated through the count chain beginning with Z4.

4.3.4.9 Detailed Troubleshooting of the First Decade

To troubleshoot the first decade, place the FUNCTION selector switch in the TEST position and the TIME BASE selector switch in the 10 s position. Observe the output of Z2 Pin 8; a 10 MHz signal should appear at Z2 Pin 8 when the GATE light is on. Observe the state of the reset at Pin 5 of Z4; when the GATE light is on, Z5 Pin 4 should be below 3 volts dc.

NOTE

A quick check of reset for proper operation can be accomplished by monitoring Z5 Pin 4 and pressing the RESET pushbutton on the front panel. When the RESET button is depressed, Pin 5 of Z4 should increase to approximately 5 volts dc. It should return to less than 3 volts when the RESET button is released.

Binary chip Z4 is a straight divide-by-two circuit. The frequency applied to Pin 6 will appear on Pin 2 divided by two. The remaining three integrated circuits are connected in a quinary configuration; Z5, Z6 and Z7 should divide the output of Z4 by five. To effectively check the operation of the individual ICs, remove Z7. The input applied to Pin 6 of Z5 will be divided by two on Pin 1. The input to Z6 Pins 6 or 9 will be divided by two again and appear on Pin 1.

To check Z7 for proper operation, insert Z7 in either Z5 or Z6 sockets and check to see if it divides by two. Replace all chips of the quinary. Z7 output will be the input applied to Z5 divided by five. The Carry amplifier, Q30 and Q31, amplifies the output of the quinary to a level capable of driving the first decade on the Count board. The output of the Carry amplifier, Pin A of the Input board, will be a signal which moves from less than 0.5 volt to greater than 3 volts of the same duty cycle as appeared at Pin 13 of Z7.

4.3.5 COUNT BOARD

NOTE

Refer to the typical accumulator section shown in Figure 4-2 when troubleshooting the Count board.

4.3.5.1 Numerical Readout Check

To scan all digits for proper numerical counting, first place the instrument in the TIME A-B position. Place the TIME BASE selector switch in the 0.1 μs position. Place the STORAGE-ON-OFF switch in the OFF position. Connect a BNC cable from the OSC OUT jack on the rear panel to the A Channel AC input jack and trigger the instrument. The instrument should now be accumulating and the most significant digit on an eight-digit instrument should be scaling at a convenient rate for visual verification of each number.

Rotate the TIME BASE selector switch to the 1 μs position. The second most significant digit should now be scaling at a convenient rate for verification of its numerical content. By rotating the TIME BASE switch in a counterclockwise direction, it will be possible to verify each number of each digit in the instrument. This simple scaling procedure allows the operator to quickly scan his entire readout, thus verifying his counter will accumulate properly.

4.3.5.2 Fault Isolation

First, perform the test in the previous paragraph. If a fault is found, note the decade in which the error occurs. The type of fault should also be noted, i.e., is a number of that decade missing, or does the counting process terminate at that decade? If a number of any certain decade is missing, the fault can be isolated to one of three elements, that is, the display tube, the decoder driver IC (7441), or the storage element IC (7475). If the instrument accumulates to a certain decade but the decades to the left of that do not receive any scaling information, investigate the decade counter IC (7490) in the decade which is inoperative.

The Count board also supplies BCD data to the rear panel through a 50-pin connector. This BCD information is generally used to drive a printer or some other form of recording instrument. If a trouble is thought to be in the BCD output, first scale to the decade which is believed to be faulty and verify that the front-panel readout for that decade is correct. If the front-panel information for that decade is proper, the fault should lie in the buffered output which takes the BCD stored information from the latch IC and buffers this information, driving the rear-panel connector.

4.3.5.3 OVERFLOW and GATE Light

The GATE indicator light is driven by a high-voltage transistor located on the Count board. The gate signal from the Function board is routed to the base of Q16 on the Count board. When the voltage on the base of Q16 reads approximately +0.7 volt dc, the GATE lamp will

light. The OVERFLOW lamp is driven by transistor Q9. A latching function is performed by the cross-coupling of NOR gates. When Z2 Pin 2 goes to the logic 1 state, the OVERFLOW lamp should light. The lamp will remain lighted until a reset pulse resets the latch.

4.3.5.4 Troubleshooting Individual Decades

When a fault is isolated to a given decade, that decade may be repaired in one of two manners. The first method of troubleshooting is the substitution of ICs. It should be noted that each circuit running from front to rear is redundant with the circuit to its right or left, therefore, IC substitutions can be made with an adjacent decade for the purpose of isolating a bad IC.

NOTE

When removing and reinstalling integrated circuits in their sockets, be careful not to bend any IC leads. A bent lead will seriously affect reliability and performance.

The second manner of troubleshooting the individual decades of the Count board is by isolating the digit as described above and checking the

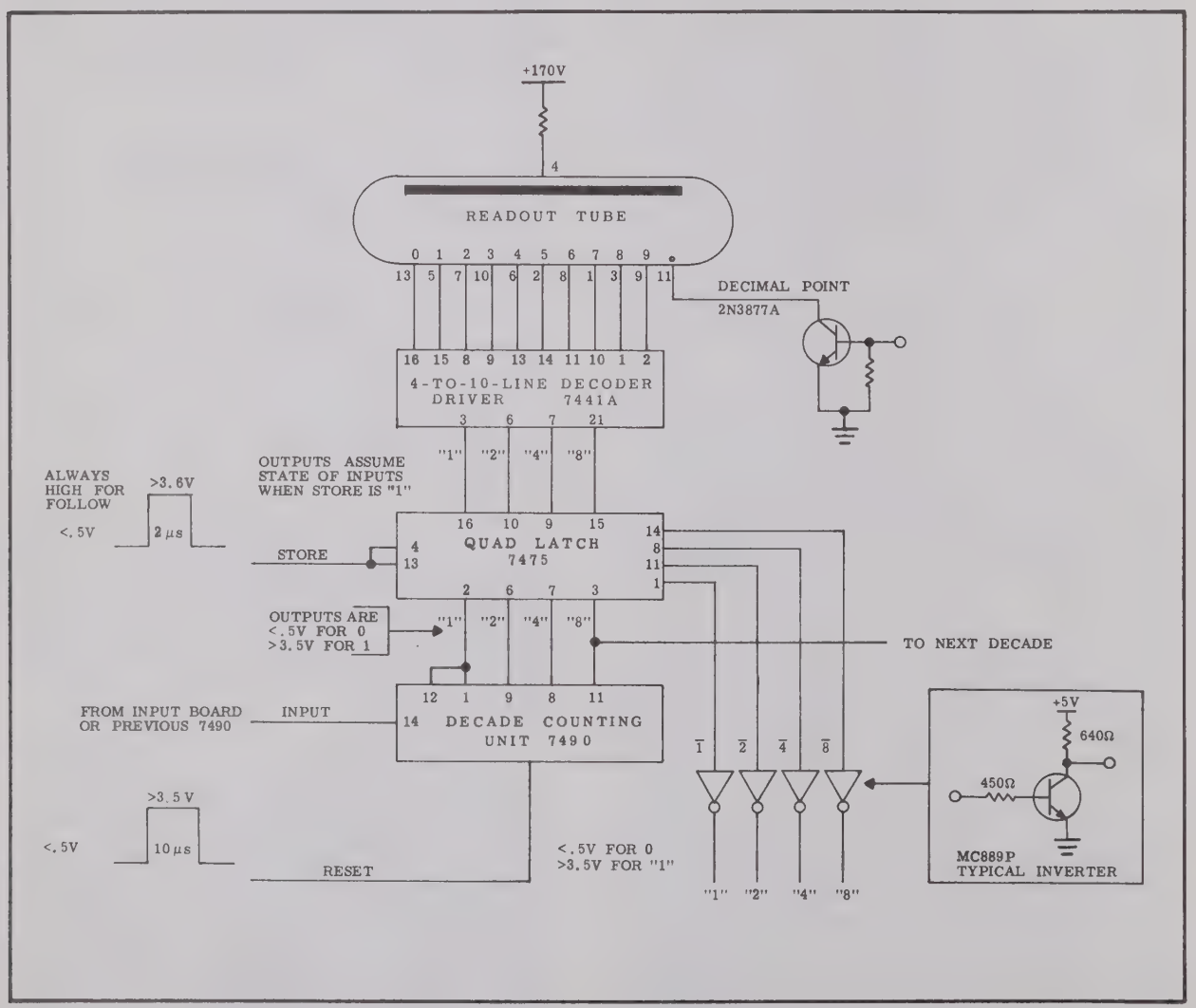


Figure 4-2. Typical Accumulator Section of the Count Board.

voltage outputs of the decade counter (7490), quad-latch (7475), and decoder driver (7441) ICs. The 1-2-4-8 outputs of the decimal counting units (7490) will all be in the LO state, i.e., less than 0.5 volt for a "0" and greater than 3.5 volts for a "1". With the instrument in the Follow mode, or Storage-Off mode, the 7475 dual-quad latch will have the same voltage on its output as it does on its input. For example, if the 7490 has a binary code "2", Pin 6 will be in the HI state; therefore, the output of the quad-latch, Pin 10, will also be in the HI state. The decoder driver will give a LO output on any pin from 0 through 9 for a given BCD code input.

EXAMPLE: If the BCD code "3" is presented to the 7475 input, pins 3 and 6 would be in the HI state on the 7475, indicating a "1" and a "2" for a BCD input of "3". Pin 9, which is the corresponding "3" output in ten-line, would be LO, thus lighting the "3" in the display tube.

4.3.6 FUNCTION BOARD

The Function board contains the decimal point, legend, recycle and time base logic sections of the counter. Before attempting to troubleshoot the Function board, first familiarize yourself with the theory of operation in the preceeding section.

The timing chart and block diagrams are intended for use as a quick reference when reading the detailed troubleshooting sections of this manual.

4.3.6.1 Decimal Point and Legend

The decimal point and legend control logic is generated on the Function board and drives the readout on the Count board. If either a decimal point or a legend character is missing from the readout, or extra decimal points or characters appear, consult the matrix, Figure 4-3, and determine which decimal point or legend character is in error. A quick check on the base of the transistor which drives the readout tube (located on the Count board) will determine if the malfunction is on the Function board. If +0.7 volt is present at the base of the drive transistor, the transistor will most likely be at

FUNCTION / TIME BASE	TEST FREQ BURST	TIME A-B PERIOD	PERIOD AVG	RATIO
10 s	DS6 / K Hz	DS4 / K S	None / μ S	DS10 ◇
1 s	DS5 / K Hz	DS2 / S	DS10 ◇ / μ S	DS9
.1 s	DS4 / K Hz	DS3 / S	DS9 / μ S	DS8
10 ms	DS3 / K Hz	DS4 / S	DS8 / μ S	DS7
1 ms	DS2 / K Hz	DS2 / m S	DS7 / μ S	DS6
.1 ms	DS4 / M Hz	DS3 / m S	DS6 / μ S	DS5
10 μs	DS3 / M Hz	DS4 / m S	DS5 / μ S	DS4
1 μs	DS2 / M Hz	DS2 / μ S	DS4 / μ S	DS3
.1 μs	n/v / n/v	DS3 / μ S	DS3 / μ S	DS2

NOTES: In COUNT/HOLD modes no decimal point or legend appears.
◇: Indicates 9th digit option only.
n/v: Indicates not valid in these positions.

Figure 4-3. Legend and Decimal Point Matrix.

fault. If no voltage is present on the base of the drive transistor, then the Function board or the interconnecting wiring between the Count and Function board will be at fault. A quick check of the voltage on the output of the integrated circuits which drive the decimal point and legend characters (located on the Function board) will isolate the trouble to either the Function board or the wire harness.

If the trouble is isolated to the Function board, check the outputs of the logic on the Function board as a starting point. Follow the signal back through the gates, using the information provided in Figure 4-3 as a reference, to determine if each gate is operating properly.

4.3.6.2 Time Base Selection

Any time base from 0.1 μs to 10 s may be selected by either a front-panel selector switch or a remote program input. The selection of the proper time base is accomplished by a contact closure to a reference voltage of less than +1 volt. The time base selected determines the decimal point position in the readout and the total number of decades required to generate a particular gate time. A change of the time base switch from one position to another is detected by integrated circuit, Z17, whose output will initiate a reset pulse.

4.3.6.3 Function Selection

The selection of any function is accomplished by a contact closure to ground by a front-panel selector switch or a remote input contact closure to ground. The function selected will determine the legend selected in the readout as well as the mode of operation for the time base and gate generation circuitry. A change of function selection will be detected by integrated circuit Z18 whose output will initiate a reset between function positions.

4.3.6.4 Slope Selection

The selection of the start and stop slope is accomplished by a contact closure to a reference voltage of less than +1 volt by either a front-panel selector switch or a remote input contact closure to ground. In either the TIME A-B or PERIOD position, the slope selector switch will enable the control of the gate by either the positive or negative-going edge of the slope of the input signal applied to the counter.

4.3.6.5 Trigger Level Lamp Drivers

The trigger level lamps are driven by the slope output driver transistors of the A and B Input Channels. The input slope applied to the trigger level lamp driver is a dc signal from approximately +0.5 volt to +5 volts dc. When the slope information is in the +0.5 to 3 volt dc region, the trigger level lamp driver transistor will be turned on, supplying +5 volts through a diode and turned-on transistor to the trigger level lamp.

4.3.6.6 Burst Control Logic

The outputs of both the A and B Channels are gated to the burst control flip-flop through channel selection gates. The A Channel information is available from a burst amplifier on the Input board. The B Channel burst information is supplied from the B positive slope information received from the Input board. The burst flip-flop, made up of gates Z28 and Z29 in a cross-coupled configuration, will be set by the introduction of an input signal on the selected channel. The setting of the burst flip-flop enables the 10 MHz reference frequency to be applied to the time base dividers. In the Burst mode, the time base will be initiated by the first pulse applied to the input amplifier.

4.3.6.7 Recycle Control Logic

NOTE

While troubleshooting the Recycle System, refer to the Timing Diagram and the Block Diagram, Figures 4-4 and 4-5, respectively.

The recycle and associated control commands will not function without a gate-closed signal from the count gate. An external signal source capable of driving TTL logic will be required to troubleshoot the recycle system. Remove Pin 6 of Z33 and connect an external signal source to Pins 1 and 2 of Z53. Adjust the output of the signal source for a pulse of approximately 10 microseconds duration. The output of the store one-shot, Pin 6 of Z53, will be a positive-going pulse, with a 5 microsecond duration. The negative transition of the storage one-shot will generate an accessory command of 10 microseconds duration on Pin 8 of Z53. Place the DISPLAY TIME switch in the MIN position. The output of Z51 will be an accessory command pulse from the accessory one-shot inverted. The negative-going output of Z51 Pin 6 will generate a reset pulse of 20 microseconds duration on Z54 Pin 4. A delayed reset pulse approximately 4 microseconds longer than the reset pulse will be present on Z54 Pin 10. Place the DISPLAY TIME switch in the VARIABLE position. In the VARIABLE display time position, the output of the accessory command one-shot triggers the display time flip-flop made up of Z56 and Z55 in a cross-coupled configuration. The output of the display flip-flop, Pin 3 of Z56, goes positive, thus allowing C2 to be charged through R9, R4, the display rate pot, and R3. When C2 becomes sufficiently charged to bring Q1 and Q2 into conduction, the collector of Q2 (which is coupled back to the display rate flip-flop) will cause the flip-flop to be reset. The reset of the display rate flip-flop will mark the end of the display time delay. The length of time that the display rate flip-flop is set will correspond to the time required to charge C2 to bring Q1 and Q2 into conduction.

4.3.6.8 Time Base Generator

To troubleshoot the individual decades of the time base divider chain, place the TIME BASE selector switch in the 10 s position. Place the FUNCTION selector switch in the TEST position. With an oscilloscope, observe the input, Pin 14, and the outputs, Pin 1, 12 and Pin 11 of each 7490 in the time base chain. With the RESET pushbutton depressed, observe the voltage state on the input pins of Z40; include Pins 3 and 11. With the RESET pushbutton depressed, the inputs to Z40 should all be in the logic 1 state.

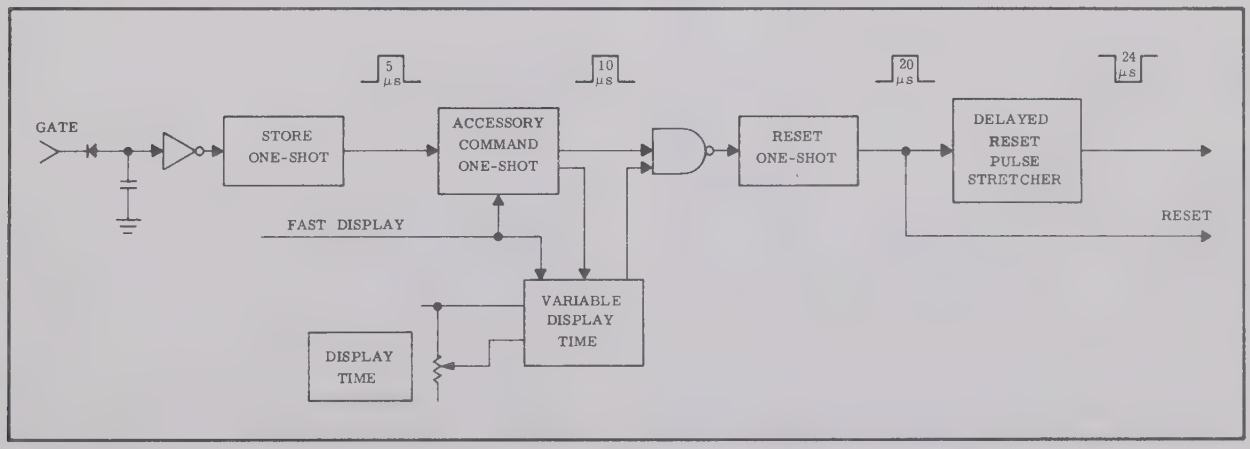


Figure 4-4. Block Diagram of the Recycle System.

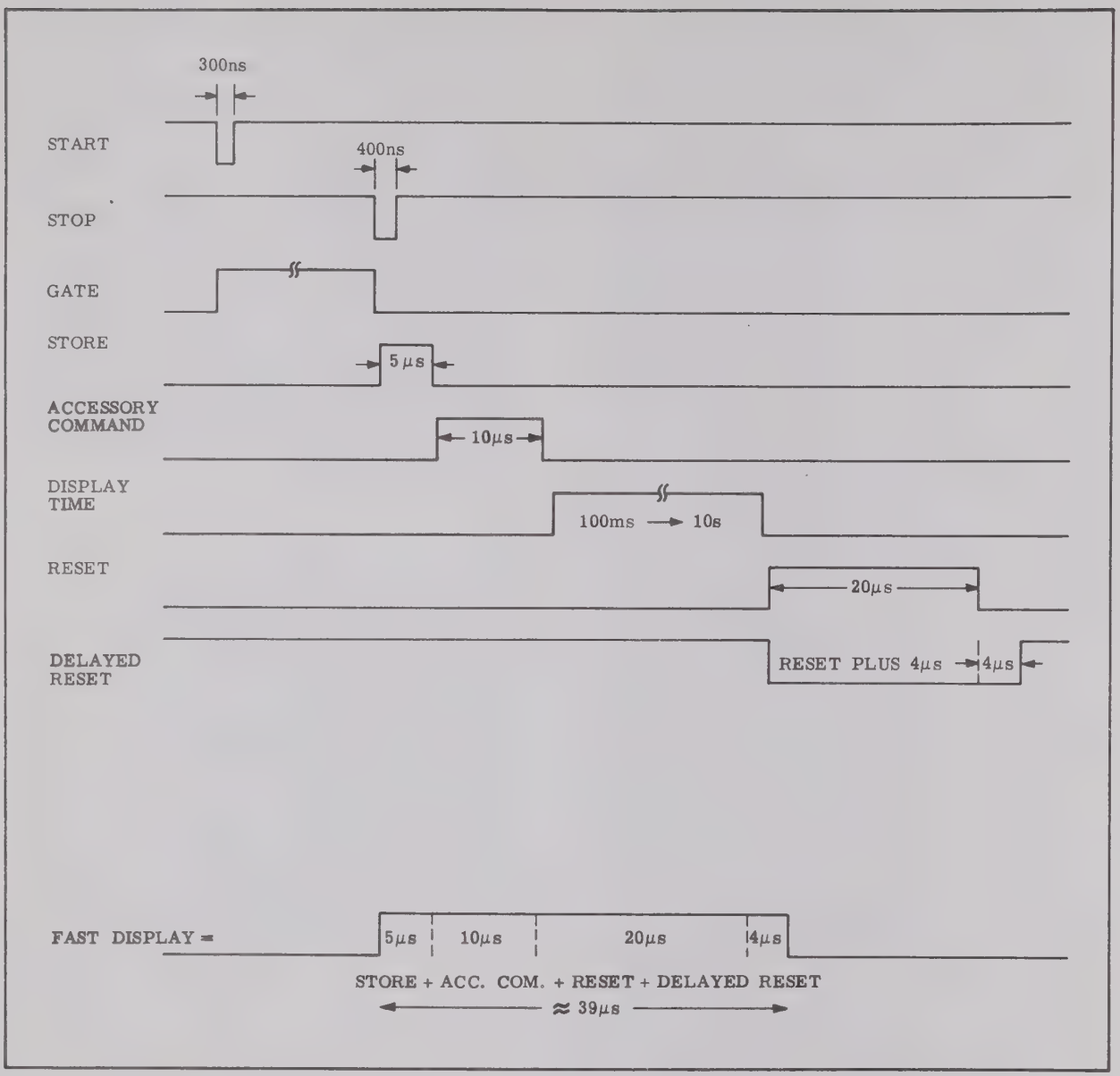


Figure 4-5. Timing Diagram.

The output, Pin 6, will be in the logic 0 state. If the output of Pin 6 is in a logic 1 state, locate the decades which are not reset. Check to see that Pin 7 of those decades are at logic 1 when reset is applied. The output of the time base comparator is applied to Pin 13 of the data logic selector IC, Z49. The output of Z49 Pin 8 will be the 10 MHz internal reference frequency in the 0.1 μs position or the output of the time base divider in the 1 μs to 10 s position. The output of the data selector is inverted by Z37 and gated by Z32 in the TEST, FREQ, BURST and RATIO mode positions to the START/STOP selector gate, Z34. The output of Z34, Pin 8, contains the start information. The positive-going edge is coupled to Pin 8 of Z31. Pin 10 of Z31 is

driven negative, setting the gate flip-flop made up of two cross-coupled NAND gates in integrated circuit Z33. When the gate flip-flop is set, a lock-out signal is sent to a second flip-flop made up of two additional cross-coupled NAND gates in Z32. If the instrument fails to gate, check to see if a start command is present.

Check the state of the lock-out flip-flop to see if it is being reset by the delayed reset signal. Pin 3 of Z32 will go negative and prevent any additional start information from being passed by Z34 Pin 9. Pin 5 of Z34 will go positive when the gate flip-flop is set. This will allow the next pulse through Z32 Pin 6 to close the count gate. The closing of the count gate by the stop pulse will generate a system recycle.

4.3.6.9 Slope Selector Circuitry

The A and B Channel slope selection logic information is applied to a logic matrix on the Function board from the selected channel and input signal slope. To select a start and a stop signal in the Period, Time A-B and Ratio modes of operation, integrated circuits Z25, Z26 and Z27 are enabled by the front-panel SLOPE and the A or B Channel select switches. The desired slope of the selected input channel is applied to Z35 for the start information and Z36 for the stop information. When troubleshooting for improper gate operation, start at Z34 Pin 8, if no stop/start pulse is present, and work backwards through Z35, then to Z25, Z26 and Z27. These ICs make up the selection matrix. The input to the matrix is channel selection, slope selection and input signal, with the combination of channel selection and slope selection producing an enabling function for gating the input signal.

If a stop pulse is missing, work back through Z34, then to Z36 and on back to Z25, Z26 and Z27.

4.3.7 POWER SUPPLY

NOTE

Refer to the Power Supply schematic diagram in Section 5 of this manual (dwg. no. D437095) while reading about troubleshooting the Regulator board.

Access to the Regulator board is provided by removing the top cover. The bottom of the Regulator board and the remaining power supply components are accessible by removing the bottom cover and the BCD board.

Apply power to the instrument and check the output of the four regulated supplies. If all four supplies are 0V, check the line voltage at the outlet into which the instrument is plugged. Check the line cord, line filter, fuse F2 and transformer T1.

CAUTION

If the fuse is replaced and immediately blows, determine the cause. DO NOT replace it with a larger value fuse.

If all four supplies are excessively high or low, check the line voltage to see that it is 120V or 240V ac ±10%. Check the 115V / 230V switch, S10, to see that it is in the appropriate position.

All four regulated supplies are similar in operation; therefore, only troubleshooting of the +15V supply will be discussed. It must be noted, however, that the +15V dc supply must be functioning correctly before proceeding with the troubleshooting of the +5V dc supply. Likewise, the +15V dc, +5V dc and -15V dc supplies must be functioning correctly before troubleshooting the +170V dc regulated supply.

The regulated supplies are all short-circuit proof and self starting when the short is removed. If the output of the +15V dc regulated supply is 0V, check the value of the unregulated

dc on filter capacitor C8, as indicated on the schematic diagram. A high value of unregulated dc voltage could indicate that no current is being supplied to the load.

A low value of unregulated dc voltage could be caused by a faulty transformer secondary, rectifier diodes, filter capacitor or excessive load on the supply.

If the unregulated voltage is normal, unsolder all of the loads at the output of the supply (terminals 10-13). If the regulated output returns to normal, replace the loads one at a time until the faulty load is isolated. If the regulated supply remains inoperative, refer to the "Theory of Operation" section for a discussion of the operation of the Regulator.

Faults in the regulator circuitry can, in most cases, be isolated by use of an ohmmeter to check for open or shorted elements of the transistors. No output from the supply could indicate an open element in transistors Q9, Q10 or Q12. An abnormally high dc voltage output with a high ripple voltage could indicate an emitter collector short in transistors Q9, Q10 or Q12.

4.4 SERVICING INTEGRATED CIRCUITS

All integrated circuits are located in sockets. The removal and substitution of identical type integrated circuits is a convenient method of troubleshooting once the problem has been isolated to a particular section of the instrument.

CAUTION

Care must be taken to insert integrated circuits correctly in the socket. Pin 1 of the IC must be inserted in Pin 1 of the socket to prevent permanent damage to the IC.

4.4.1 SPECIAL TROUBLESHOOTING PROCEDURES

The following special troubleshooting procedures are recommended for instruments using integrated circuits.

1. Be sure that the ground terminals or chassis of all line-operated test equipment are solidly and securely connected to instrument ground.
2. Use small pin-tipped test probes on meters and oscilloscopes to reduce the chance of shorting IC leads together.
3. Even though the power supplies cannot be damaged, use the greatest care to avoid even a momentary short of any point in a circuit to ground or to other circuit points, to prevent damage to components.
4. Do not allow "dangling" oscilloscope probe ground leads, or other stray leads, to touch circuitry in the instrument.
5. Unplug the line cord before removing or replacing components.

4.4.2 DESCRIPTION OF LOGIC ELEMENTS

Use the logic symbols and equations defined in Figure 4-6 to interpret the logic diagrams and truth tables listed in Table 4-1.

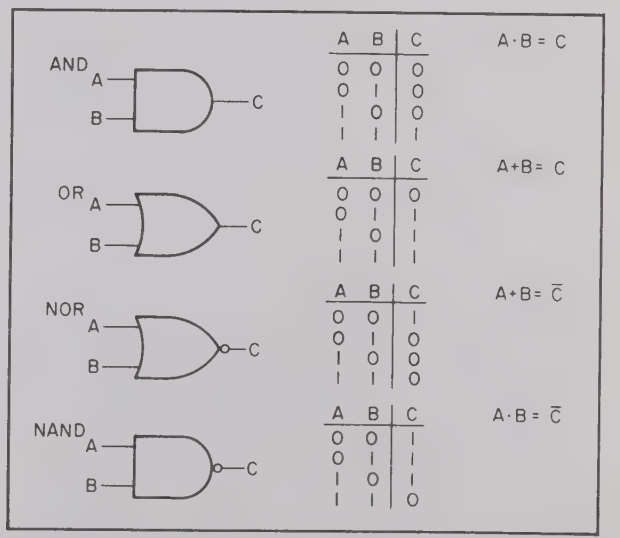


Figure 4-6. Logic Symbols and Truth Tables.

Table 4-1. Integrated Circuit Logic Diagrams and Truth Tables

Type	Number	Description	Figure No.	Beckman No.
RTL	MC 889	Hex Inverter	4-7	885-857580
ECL	MC 1010	Quad Two-Input NOR Gate	4-8	885-857591
ECL	MC 1013	70 MHz Flip-Flop	4-9	885-435259
ECL	MC 1023	Four-Input Clock Driver	4-10	885-857589
ECL	MC 1034	Type "D" Flip-Flop	4-11	885-857537
DTL	830	Dual Four-Input NAND Gate	4-12	885-846631
DTL	837	Hex Inverter	4-13	885-846628
DTL	846	Quad Two-Input NAND Gate	4-14	885-846627
DTL	862	Triple Three-Input NAND Gate	4-15	885-846625
TTL	3374	25 MHz Counters	4-16	885-857579
TTL	7400	Quad Two-Input NAND Gate	4-14	885-857583
TTL	7402	Quad Two-Input NOR Gate	4-17	885-857538
TTL	7410	Triple Three-Input NAND Gate	4-15	885-857582
TTL	7441A or 74141	BCD-To-Decimal Decoder	4-18	885-857578
TTL	7450	Dual Two-Wide Two-Input AND-OR-INVERTER	4-19	885-857555
TTL	7475	Quadruple Bistable Latch	4-20	885-857576
TTL	7490	10 MHz Counters	4-16	885-857577
HTTL	74H10	Triple Three-Input NAND Gate	4-15	885-857584

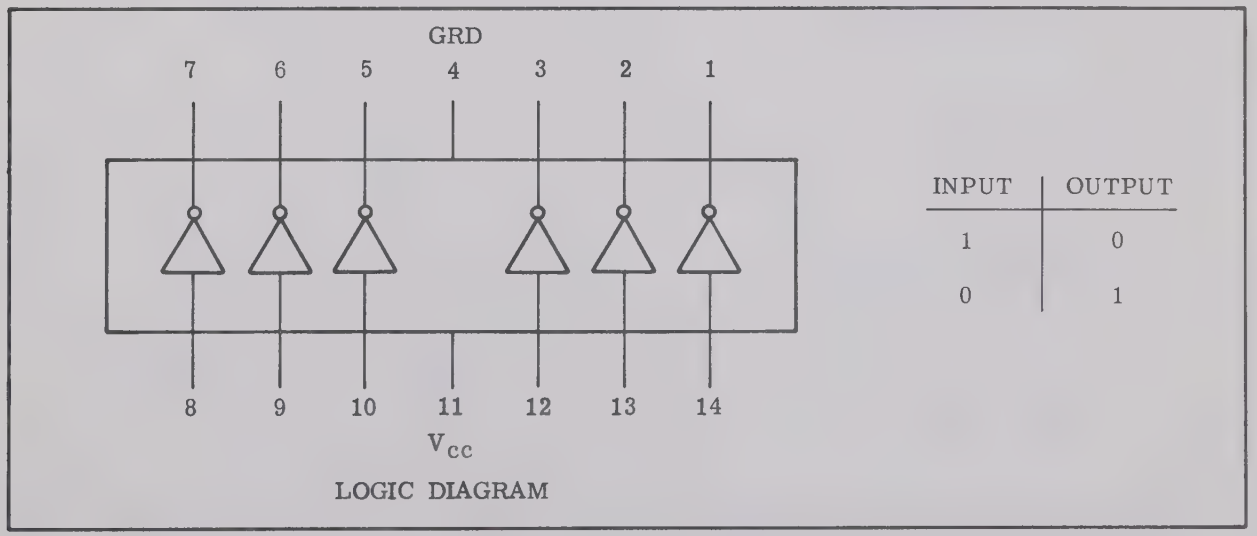
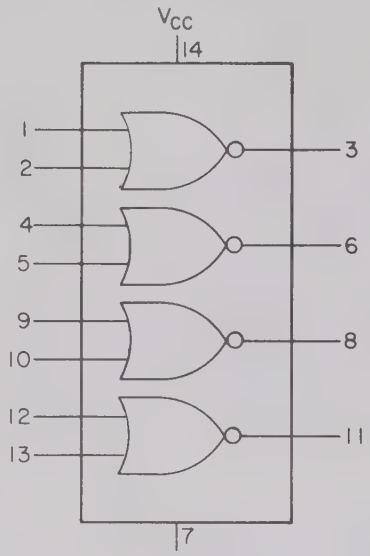


Figure 4-7. Logic Diagram, Hex Inverter.

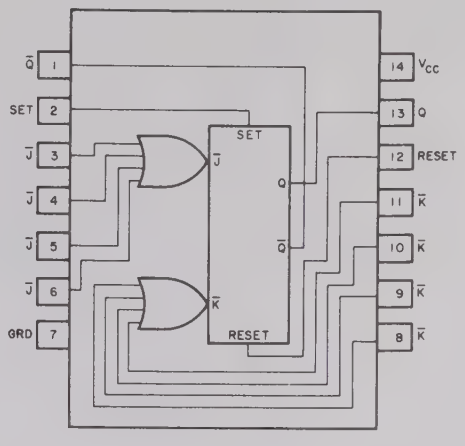
LOGIC DIAGRAM



A	B	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	0

(A and B are inputs)

Figure 4-8. Quad Two-Input NOR Gate.



CLOCK $\overline{J}$-$\overline{K}$
TRUTH TABLE

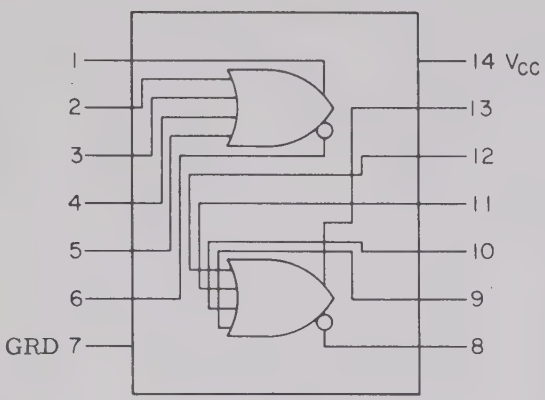
	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^n
PIN NO.	*	*	**	13
	Ø	Ø	0	Q^n
	0	0	1	$\overline{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

NOTES

1. All other $\overline{J}$-$\overline{K}$ inputs and the R-S inputs are at a "0" level.
2. *Any one of the $\overline{J}$ or $\overline{K}$ inputs may be used.
3. **Any $\overline{J}$ and $\overline{K}$ inputs may be tied together to form C_D (Example pins 6 and 8).

Figure 4-9. 70 MHz Flip-Flop.

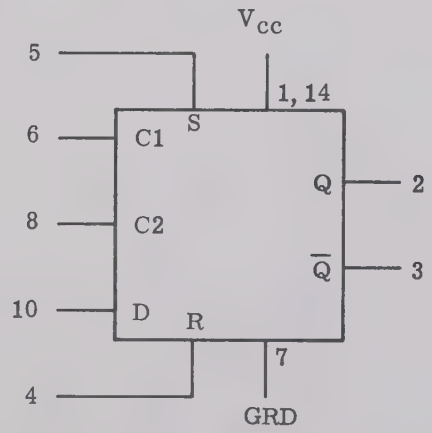
LOGIC DIAGRAM



INPUTS	OUTPUT PINS 6 OR 8	OUTPUT PINS 1 OR 13
A+B+C+D = 1	0	1
A·B·C·D = 0	1	0

(A,B,C,D are inputs)

Figure 4-10. Four-Input Clock Driver.



continued

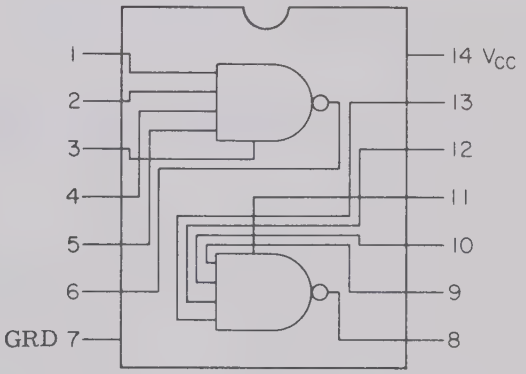
CLOCKED TRUTH TABLE

D	C	Q^{n+1}	$\overline{Q}^{n+1}$
10	6 or 8	2	3
0	0	Q^n	$\overline{Q}^n$
1	0	Q^n	$\overline{Q}^n$
0	1*	0	1
1	1*	1	0

*A "1" or Clock input is defined for this flip-flop as a change in level from a low state to a high state of the clock.

Figure 4-11. Type "D" Flip-Flop.

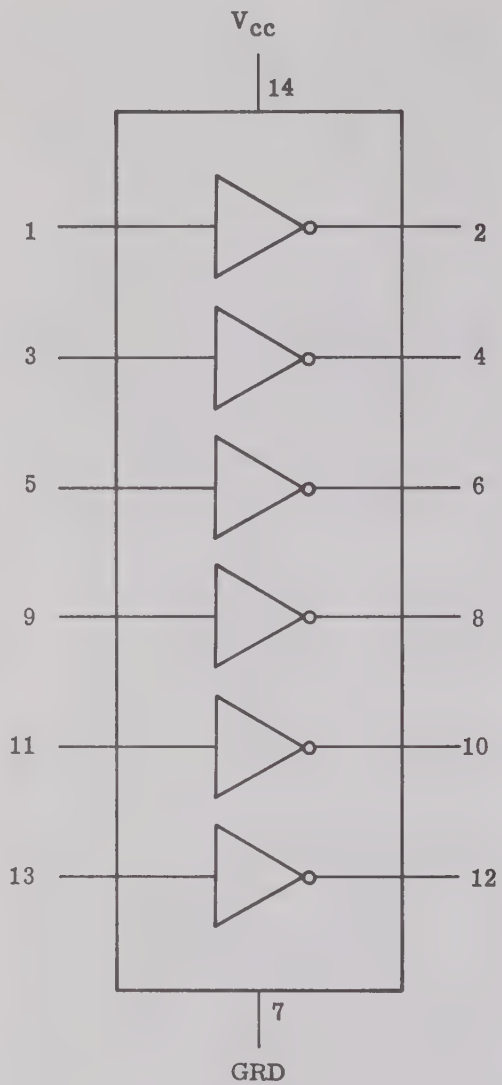
LOGIC DIAGRAM



INPUTS	OUTPUT
A·B·C·D = 1	0
A+B+C+D = 0	1

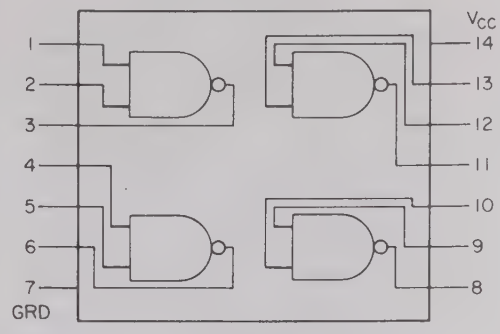
(A,B,C,D are inputs)

Figure 4-12. Dual Four-Input NAND Gate.



INPUT	OUTPUT
1	0
0	1

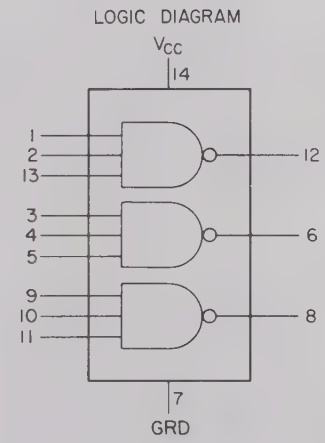
Figure 4-13. Hex Inverter.



A	B	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

(A and B are inputs)

Figure 4-14. Quad Two-Input NAND Gate.

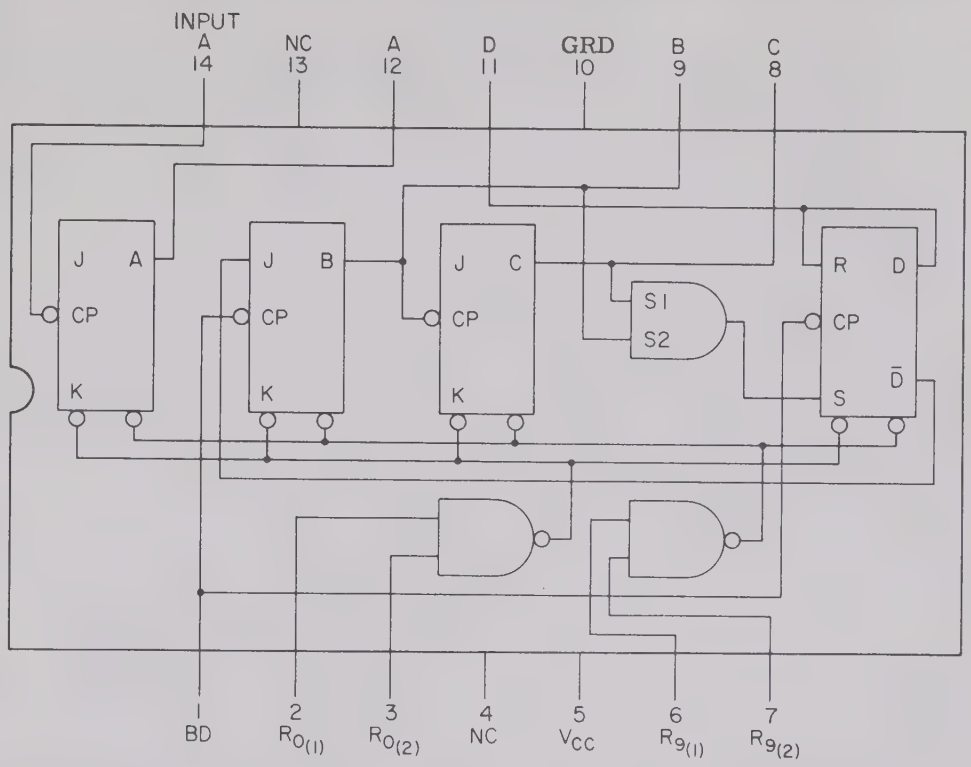


INPUTS	OUTPUT
A·B·C = 1	0
A+B+C = 0	1

(A,B,C are inputs)

Figure 4-15. Triple Three-Input NAND Gate.

LOGIC DIAGRAM



BCD COUNT SEQUENCE

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

See Note 1

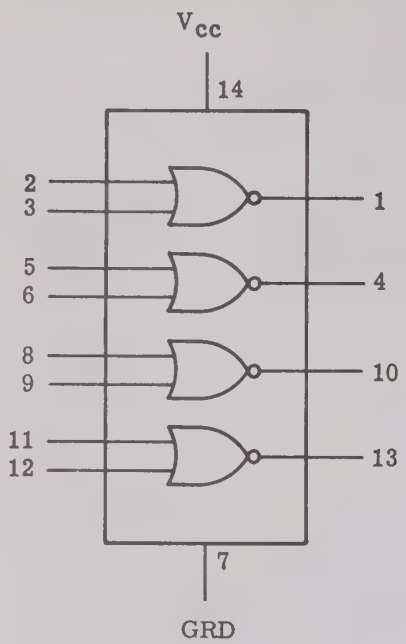
RESET/COUNT

RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

See Note 2

NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

Figure 4-16. 10 and 25 MHz Counters



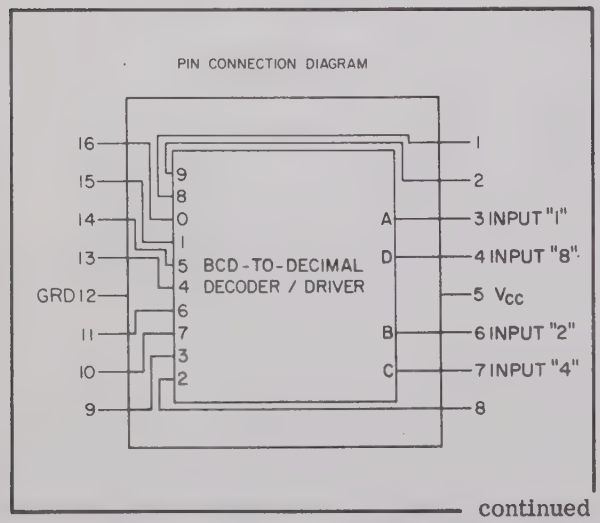
AB	OUTPUT
00	1
01	0
10	0
11	0

Figure 4-17. Quad Two-Input NOR Gate.

INPUT				OUTPUT
D	C	B	A	ON
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

All other outputs are off.

Figure 4-18. BCD-To-Decimal Decoder.



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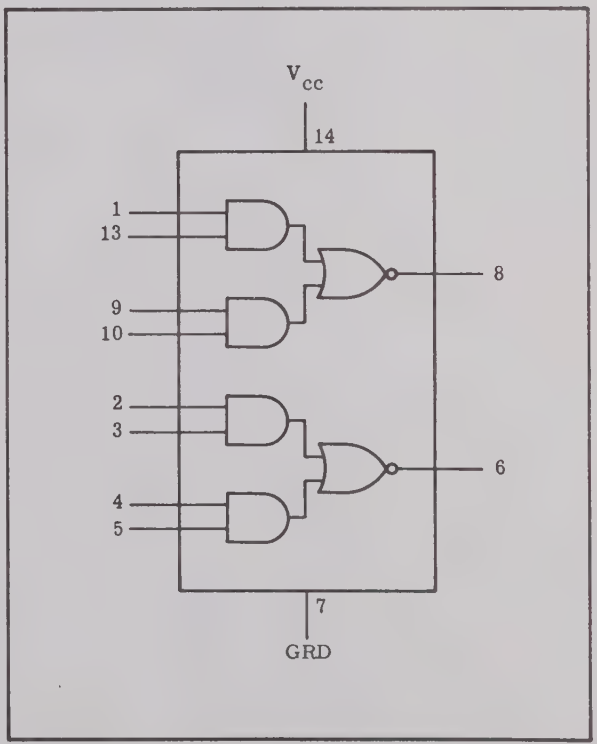
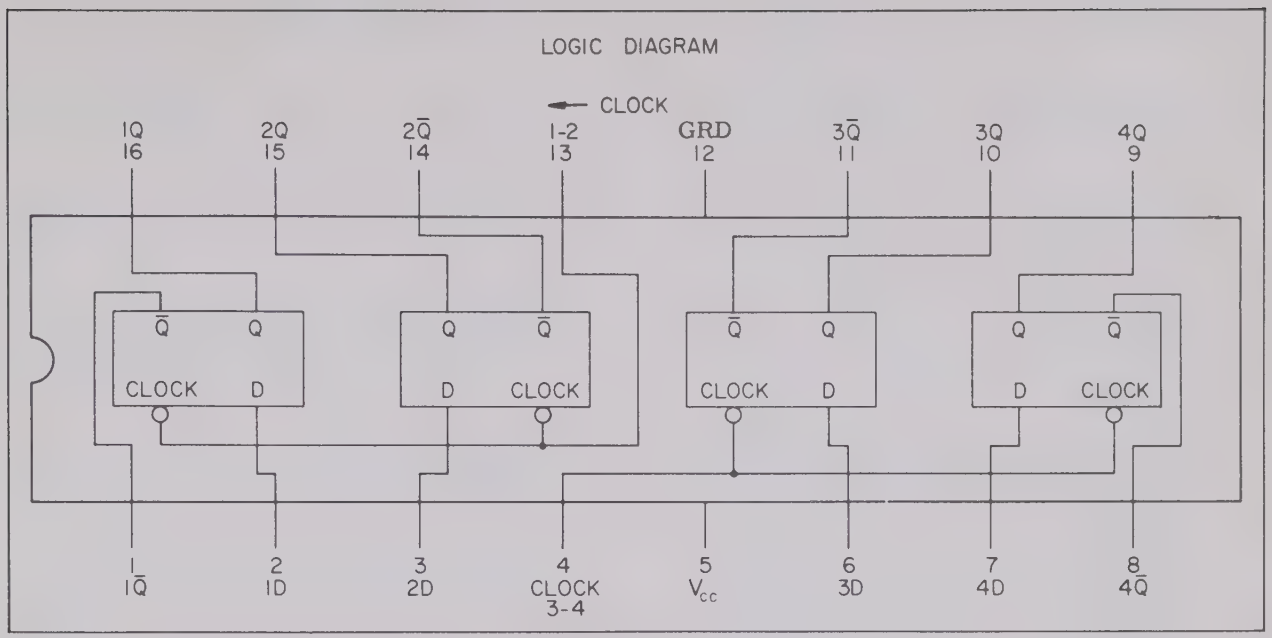


Figure 4-19. Dual Two-Wide Two-Input AND-OR-Inverter.



TRUTH TABLE
(Each Latch)

t_n	t_{n+1}	
D	Q	$\overline{Q}$
1	1	0
0	0	1

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

Figure 4-20. Quadruple Bistable Latch.

4.5 ADJUSTMENTS

4.5.1 PRESET TRIGGER

To adjust the preset trigger, follow these recommended procedures:

1) Place the FUNCTION selector switch in the PERIOD AVG position.

2) Place the TIME BASE selector switch in the 1 ms position.

3) Connect an ac signal source to the A input and set the frequency to 11 MHz at 80 mV rms.

4) Place the trigger control pot in the (P) position.

5) Adjust the preset trigger pot R12 for proper counting.

6) Decrease the input amplitude and readjust the pot until the best sensitivity for proper counting is achieved.

7) Place the A attenuator switch in the B INPUT position and connect the signal source to the B Channel.

8) Proceed as above by adjusting R50 for the B Channel.

4.5.2 POWER SUPPLY

Refer to Section 5 for location of the test points and potentiometers of the regulated power supply. Proceed in sequence as follows when making these adjustments:

1) Monitor the -15V test point, terminals 6 through 9.

2) Adjust potentiometer R39 to obtain -15V dc ±150 millivolts.

3) Monitor the +15V test point, terminals 10 through 13.

4) Adjust potentiometer R29 to obtain +15V dc ±150 millivolts.

5) Monitor the +5V test point, terminals 14 through 17.

6) Adjust potentiometer R19 to obtain +5V dc ±50 millivolts.

7) Monitor the +170V test point, terminal 5.

8) Adjust potentiometer R7 to obtain +170V dc ±1.7 volts.

MODEL 6401-O

4.5.3 OSCILLATOR AND MULTIPLIER

The oscillator frequency may be set by comparing it to a frequency standard. The adjustment is accessible through a hole in the rear panel.

The following equipment (or its equivalent) will be required for calibration and adjustment of the 1, 2.5, 5 MHz to 10 MHz Oscillator and Multiplier. (See diagrams in Section 5 of this manual.)

- Calibrated oscilloscope, Model 581 with 82 Plug-in; 10:1 probe.
- 1 MHz standard (with drift rate less than 5×10^{8} per 24 hours) 1 volt rms amplitude.

To make the initial adjustments, follow this procedure:

1) Set oscillator to nominal frequency.

2) Connect scope probe to junction of R4 (5.6K) and Q2 (source).

3) Connect 1 MHz standard to scope EXT-HORIZ IN and adjust scope horizontal and vertical gain for centered Lissajou pattern.

4) Adjust C1 (on oscillator) for a reasonably stationary pattern (minimum rotational drift).

5) Adjust oscillator amplitude to 3 volts peak-to-peak.

6) Return scope to NORMAL - HORIZONTAL-SWEEP; Time base to 0.1 μs cm; Vertical sensitivity to 1 volt/cm and adjust R3 for 3 volts peak-to-peak at oscillator frequency.

7) Repeat steps 3 and 5. There is a slight interaction between adjustments.

8) Adjust 10 MHz multiplier and tank circuit (rear-panel switch in OSC OUT position).

9) Move scope probe to junction of R17 (820Ω) and Q7 collector.

10) Adjust C13 for a maximum amplitude 10 MHz signal.

11) Adjust C12 for best symmetry (i.e., 50% duty cycle of 10 MHz signal).

If an external frequency is to be used, proceed as follows:

1) Set rear-panel switch to REF-FREQ-IN position and apply 1 MHz standard to OSC OUT jack (J8).

2) Adjust fine tuning on C12 and C13 as required to achieve a 3 volt peak-to-peak, symmetrical, jitter-free 10 MHz output.

3) Switch S8 back and forth several times from OSC OUT to REF-FREQ-IN, adjusting C12 and C13 to achieve a correct, jitter-free 10 MHz signal in both positions of switch.

4) Remove the external standard from J8.

5) Place S8 in the OSC OUT position.

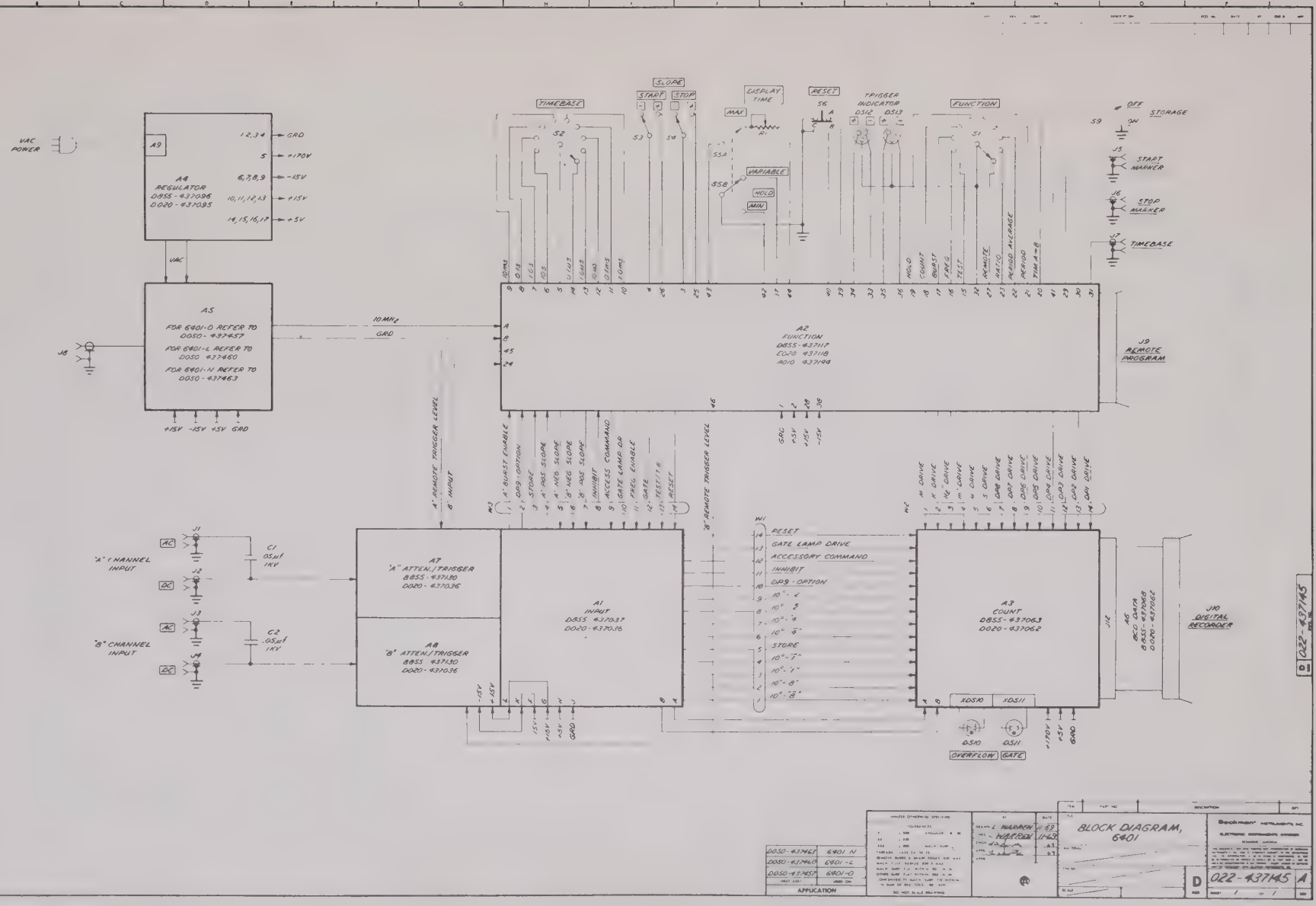
6) Connect scope probe to J8 to verify that a buffered 10 MHz output is present.

SECTION 5. PARTS LISTS & DIAGRAMS

Description	Dwg. No.	Page
Block Diagram	D437145 (A)	5-1
Outline Drawing	C437151 (A)	5-2
Basic Assembly	D437455 (A)	5-3
Mechanical & Wired Assembly	D437453 (A)	5-4
Input Board (A1) Component Layout	D437037 (D)	5-5
Parts List		5-6
Schematic (2 pages)	D437036 (D)	5-8
Function Board (A2) Component Layout	D437117 (D)	5-10
Parts List		5-11
Schematic	E437118 (B)	5-13
Count Board (A3) Component Layout	D437063 (F)	5-15
Parts List		5-16
Schematic	D437062 (E)	5-17
Regulator Board (A4) Assembly	D437096 (E)	5-18
Parts List		5-19
Schematic	D437095 (C)	5-21
Atten/Trigger Switch (A7, A8) Component Layout with Parts List	B437130 (A)	5-22
Front Panel Mechanical & Wired Assembly	C437126 (A)	5-23
Rear Panel Mechanical & Wired Assembly	C437133 (C)	5-24
Parts List: Miscellaneous		5-25

MODEL 6401-O

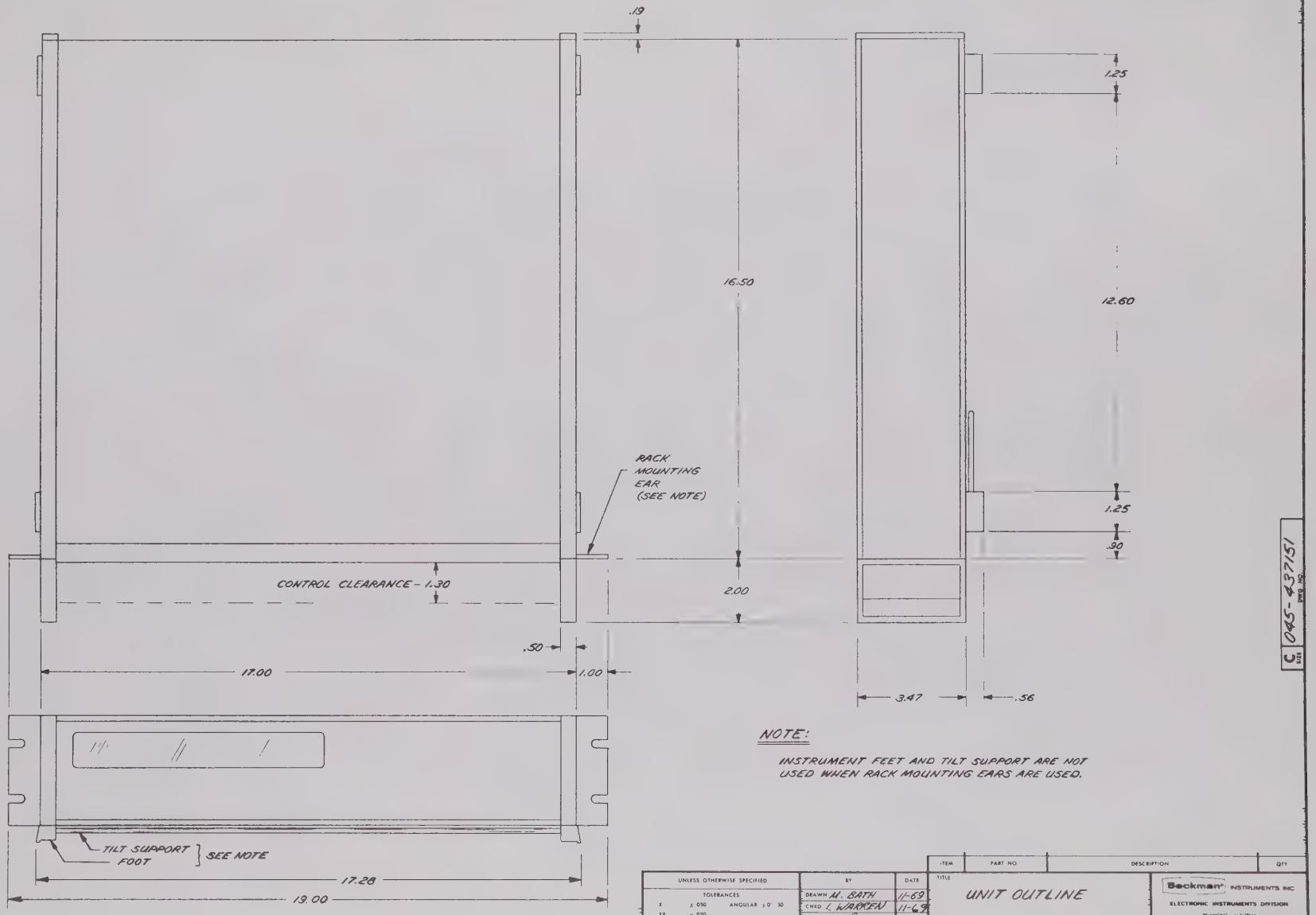
Oscillator Board (A5) Component Layout	C437355 (A)	5-26
Parts List		5-27
Schematic	D437359 (A)	5-29
Final Assembly	D437457 (A)	5-30



APPLICATION	
D050-437457	6401-N
D050-437460	6401-L
D050-437457	6401-O

BLOCK DIAGRAM, 6401

022-437145 A



NOTE:

INSTRUMENT FEET AND TILT SUPPORT ARE NOT USED WHEN RACK MOUNTING EARS ARE USED.

ZONE	REV	BY	DESCRIPTION	ECO No	DATE	BY	CHK'D	APP'D

ITEM	PART NO	DESCRIPTION	QTY

APPLICATION	
NEXT ASSY	USED ON
A037-437469	6401-N
A037-437461	6401-L
A037-437458	6401-O

UNLESS OTHERWISE SPECIFIED
TOLERANCES
X ± .050 ANGULAR ± 0° 30'
XX ± .020
XXX ± .005 MACH SURF ✓
THREADS CLASS 3A OR 3B
REMOVE BURRS & SHARP EDGES .020 MAX
MACH FILET RADIUS .020 R MAX
MACH SURF FLAT WITHIN .001 IN IN
OTHER SURF FLAT WITHIN .003 IN IN
CONCENTRICITY MACH SURF TIR WITHIN ½ SUM OF DIA TOLS, .001 MIN
DO NOT SCALE DRAWING

	BY	DATE
DRAWN	M. BATH	11-69
CHK'D	L. WARREN	11-69
ENGR		11-69
APP'D		11-69
APP'D		

TITLE: UNIT OUTLINE

MATERIAL

FINISH

SCALE 1 : 2

SIZE C

Beckman® INSTRUMENTS, INC
ELECTRONIC INSTRUMENTS DIVISION

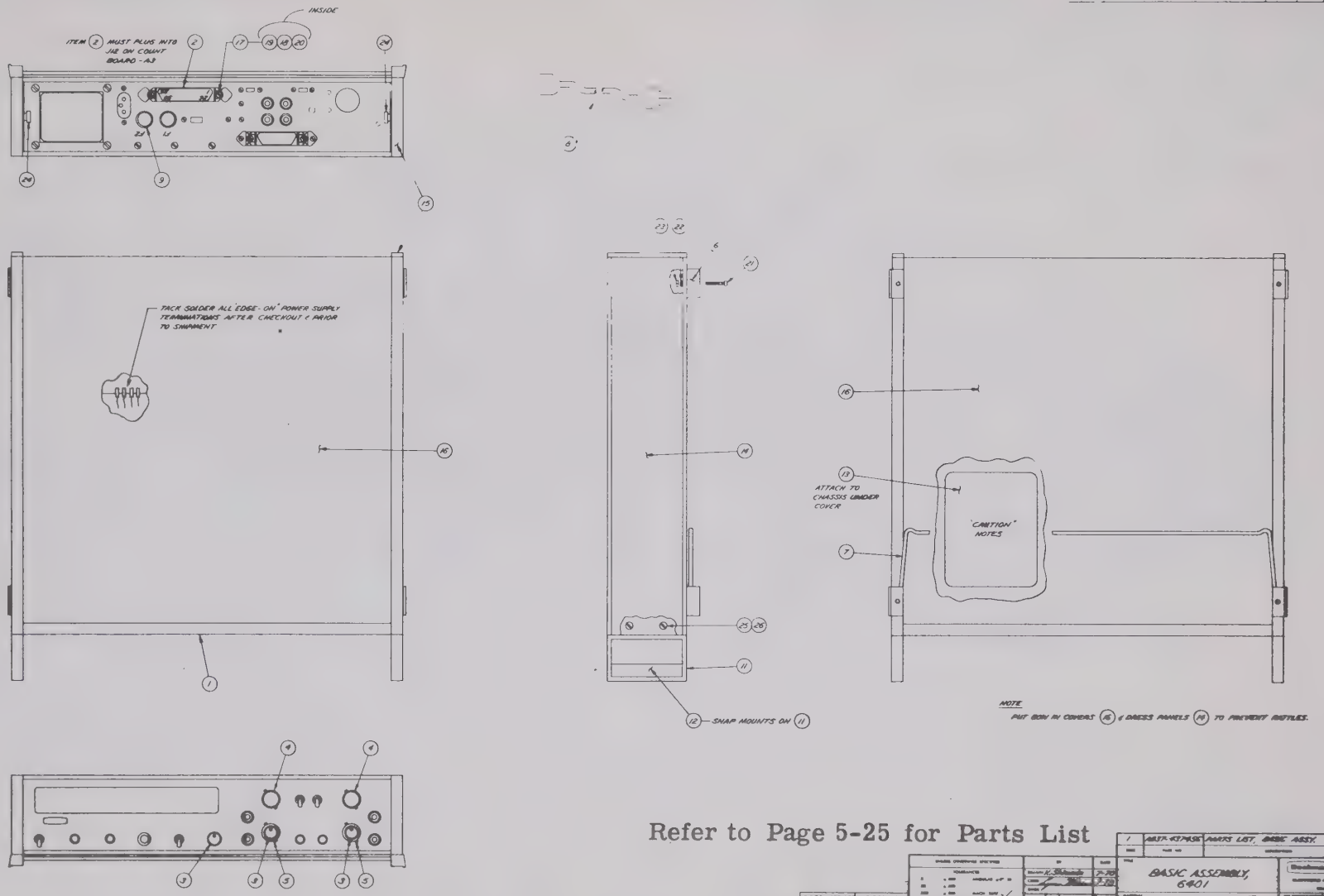
045-437151 A

SHEET 1 OF 1

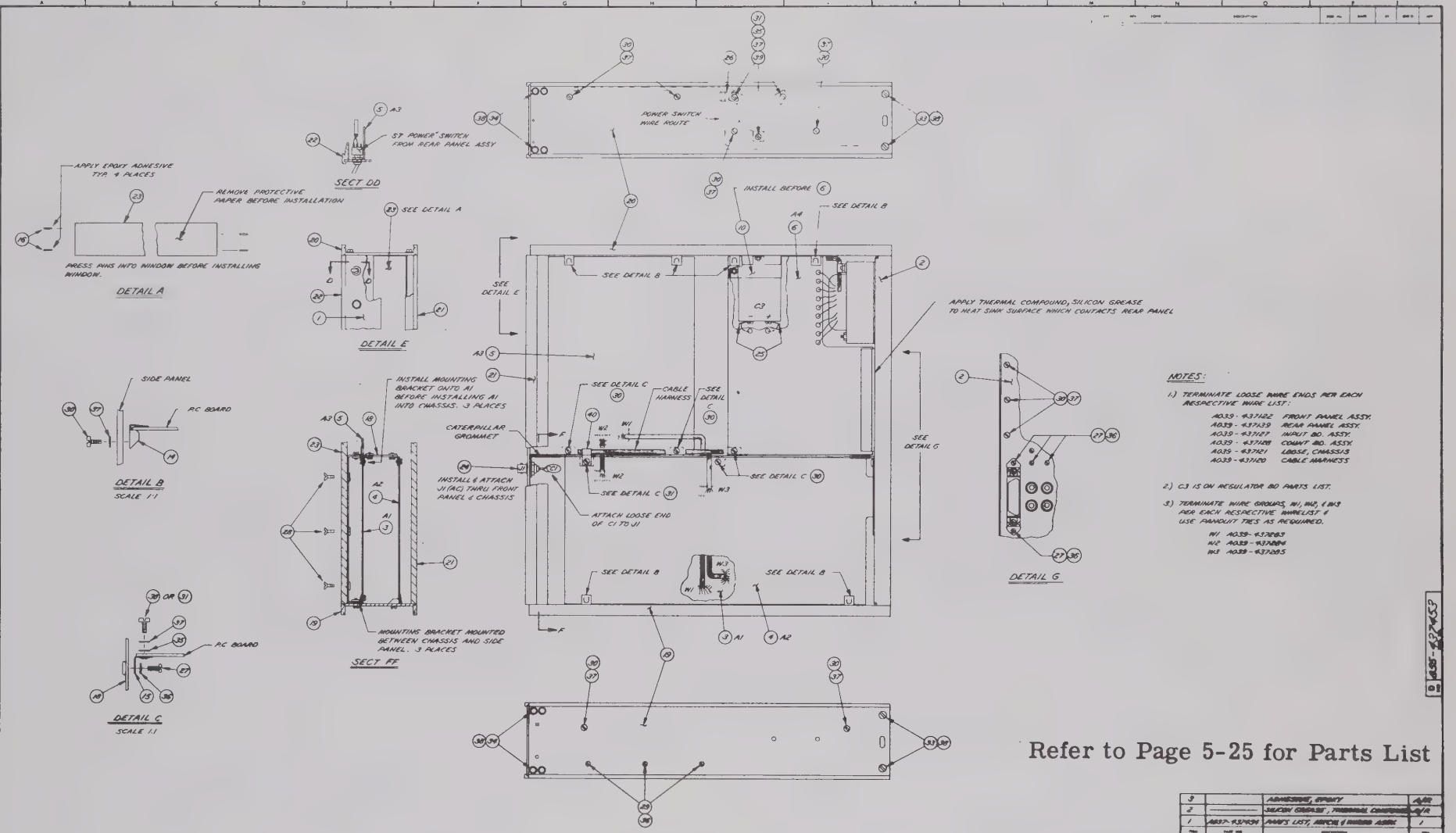
C 045-437151

ED-013

00

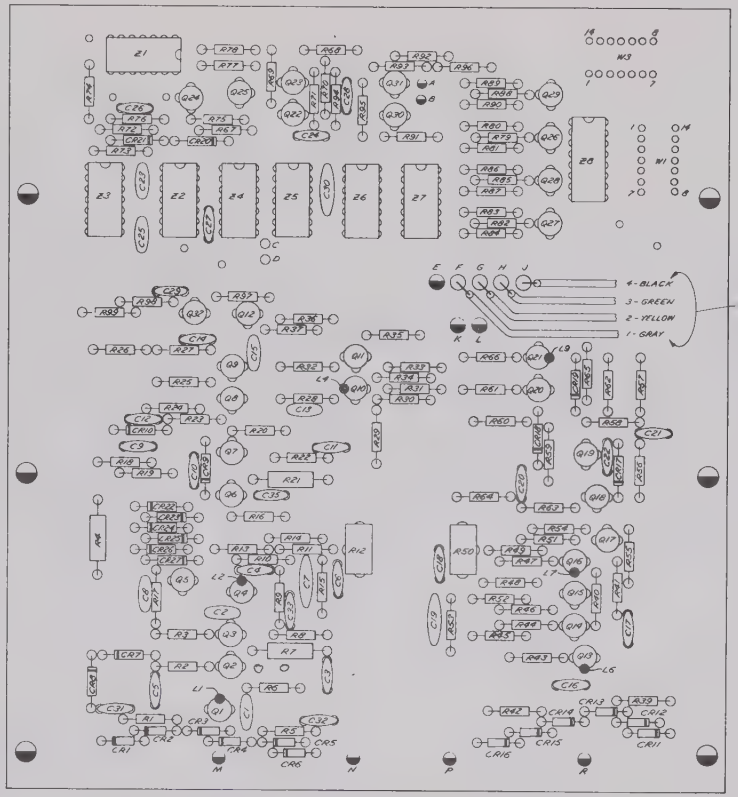

INSIDE
ITEM (2) MUST PLUG INTO J12 ON COUNT BOARD - A3
TACK SOLDER ALL 'EDGE - ON' POWER SUPPLY TERMINATIONS AFTER CHECKOUT & PRIOR TO SHIPMENT
ATTACH TO CHASSIS UNDER COVER
"CAUTION" NOTES
SNAP MOUNTS ON (11)
NOTE
PUT BOW IN COVERS (16) & DRESS PANELS (18) TO PREVENT RATTLES.
BASIC ASSEMBLY, 6401
6333-437455

Refer to Page 5-25 for Parts List


APPLY FRONT ADHESIVE TYP. 4 PLACES
REMOVE PROTECTIVE PAPER BEFORE INSTALLATION
PRESS PINS INTO WINDOW BEFORE INSTALLING WINDOW.
DETAIL A
SECT DD
S7 POWER SWITCH FROM REAR PANEL ASSY
SEE DETAIL A
DETAIL E
POWER SWITCH WIRE ROUTE
INSTALL BEFORE 6
SEE DETAIL B
SEE DETAIL E
SEE DETAIL B
C3
APPLY THERMAL COMPOUND, SILICON GREASE TO HEAT SINK SURFACE WHICH CONTACTS REAR PANEL
SEE DETAIL G
SIDE PANEL
PC BOARD
DETAIL B
SCALE 1:1
INSTALL MOUNTING BRACKET ONTO A1 BEFORE INSTALLING A1 INTO CHASSIS. 3 PLACES
CATERPILLAR GROMMET
CABLE HARNESS
SEE DETAIL C
INSTALL & ATTACH J1 (AC) THRU FRONT PANEL & CHASSIS
ATTACH LOOSE END OF C1 TO J1
SEE DETAIL C
SEE DETAIL B
SEE DETAIL B
A1
A2
MOUNTING BRACKET MOUNTED BETWEEN CHASSIS AND SIDE PANEL. 3 PLACES
SECT FF
DETAIL G
NOTES:
1.) TERMINATE LOOSE WIRE ENDS PER EACH RESPECTIVE WIRE LIST:
A039-937162 FRONT PANEL ASSY.
A039-937139 REAR PANEL ASSY.
A039-937127 INPUT BD. ASSY.
A039-937128 COUNT BD. ASSY.
A035-937121 LOOSE, CHASSIS
A039-937120 CABLE HARNESS
2.) C3 IS ON REGULATOR BD PARTS LIST.
3.) TERMINATE WIRE GROUPS W1, W2, & W3 PER EACH RESPECTIVE WIRELIST # USE PANDUIT TIES AS REQUIRED.
W1 A039-937083
W2 A039-937084
W3 A039-937085
DETAIL C
SCALE 1:1
P.C. BOARD
OR
MECH. & WIRED ASSY, 6401 BASIC
A035-937453
APPLICATION

Refer to Page 5-25 for Parts List

B		COMPONENT RELAYOUT	12388	12-69	L W	
C		SEE ECO	12293	3-70	KAE	



NOTES:

1. ● - INDICATES FERRITE BEAD ON TRANSISTOR LEAD.
2. ◒ - INDICATES HOLES TO BE MASKED PRIOR TO SOLDERING.
3. Z1-Z8 ARE SOCKET MOUNTED
4. SPECIAL PREPARATION REQUIRED FOR CR1,2,3,4,5,6,11,12,13,14,15,16 NON-STANDARD SPACING
5. INSERT WIRES PRIOR TO SOLDERING OPERATION WIRE LIST A039-637127
6. L1, L2, L6 & L7 MUST BE INSULATED TO PREVENT THEM FROM TOUCHING ADJACENT TRANSISTOR LEADS
   TYPICAL FOR 4 LEADED TRANSISTORS; REMOVE LEAD SHOWN:

7. INSTALL WIRE GROUPS 'W1' & 'W3' AFTER WAVE SOLDER OPERATION PER WIRE LISTS:
   W1 - A039-637283
   W3 - A039-637285

2	0020-637036	SCHEMATIC INPUT BOARD	REF.
1	A037-637035	PARTS LIST, INPUT BD	1

855-637192	6401
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
TOLERANCES
DRAWN K. Shimada 8/69
CHKD
ENGR
APPD
MFG
MATERIAL
FINISH
SCALE 2:1
P.C. BOARD ASSY, INPUT-A1
Tektronix, Inc. ELECTRONIC PRODUCTS DIVISION
DO NOT SCALE DRAWING
855-637037 D
SHEET 1 OF 1

855-637037 D

INPUT BOARD ASSEMBLY (A1) - PARTS LIST

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty./ Assy.
	D-437037-D	Input Board (A1)	Beckman	
C1, 25	637-822251	Capacitor, F. Mica, 100pf, 500V, 5%	*DM15-F101J0-WV4CR	2
C2, 13, 26	637-825071	Capacitor, F. Mica, 27pf, 500V, 5%	DM15-E270J0-WV4CR	3
C3, 5, 6, 9, 10, 11, 12, 14, 17, 18, 20, 21, 22, 24, 28, 29, 31, 32, 33	633-836864	Capacitor, F. Cerm., 0.01μf, 100V	Sprague C023B101F-103M	19
C4, 16, 27	633-857571	Capacitor, F. Cerm., 47pf	Sprague 5GA-Q47	3
C7, 19, 30	633-815873	Capacitor, F. Cerm., 0.33μf, 25V	Sprague 5C023334D-8250B3	3
C8, 23, 35	637-825069	Capacitor, F. Mica, 10pf, 500V, 5%	DM15-C100J0-WV4CR	3
C15	637-857581	Capacitor, F. Mica, 6pf, 500V, 5%	DM15-C060D0-WV4CR	1
CR1, 2, 3, 4, 5, 6, 7, 11, 12. 13, 14, 15, 16, 20 thru 27	755-838731	Diode, 1N4448	Continental Devices	21
CR8, 18	755-832774	Diode, Zener, 8.2V, 5%, 1N756A	Motorola	2
CR9	755-814019	Diode, Zener, 6.8V, 5%, 1N754A	Motorola	1
CR10	755-818496	Diode, Zener, 5.1V, 5%, 1N751A	Motorola	1
CR17	755-822858	Diode, Zener, 6.2V, 5%, 1N753A	Continental Devices	1
CR19	755-836043	Diode, Zener, 12.0V, 5%, 1N759A	Motorola	1
L1, 2, 4, 6, 7, 9	783-807862	Ferrite Bead	Ferroxcube 56-590-65/3B	6
Q1 & Q4, Q13 & Q16	755-857548	Transistor, Matched Pair	Tex. Instr. TIS69	2 pr.
Q2, 3	755-857328	Transistor, 40235	RCA	2
Q5, 8, 9, 12, 17, 22, 23, 25, 26, 27, 28, 29, 30, 31, 32	755-845089	Transistor, 2N4258	Fairchild	15
Q6, 7	755-857419	Transistor, 2N5179	RCA	2
Q10, 11, 14, 15, 18, 19, 20, 21, 24	755-857274	Transistor, 2N4275	Fairchild	9
R1, 5, 39, 42, 45	601-822295	Resistor, 2.7K, 1/4W, 5%	**A. B. CB2725	5
R2, 3, 10, 56, 58, 69, 73, 76, 81, 84, 87, 90	601-823394	Resistor, 330Ω, 1/4W, 5%	A. B. CB3315	12
R4	601-015442	Resistor, 150Ω, 1/2W, 5%	A. B. EB1515	1
R6, 9, 43, 47	601-823902	Resistor, 47K, 1/4W, 5%	A. B. CB4735	4
R7, 21	601-008129	Resistor, 1.5K, 1/2W, 5%	A. B. EB1525	2
R8, 20, 64	601-817735	Resistor, 100Ω, 1/4W, 5%	A. B. CB1015	3
R11	601-823397	Resistor, 5.6K, 1/4W, 5%	A. B. CB5625	1

continued. . .

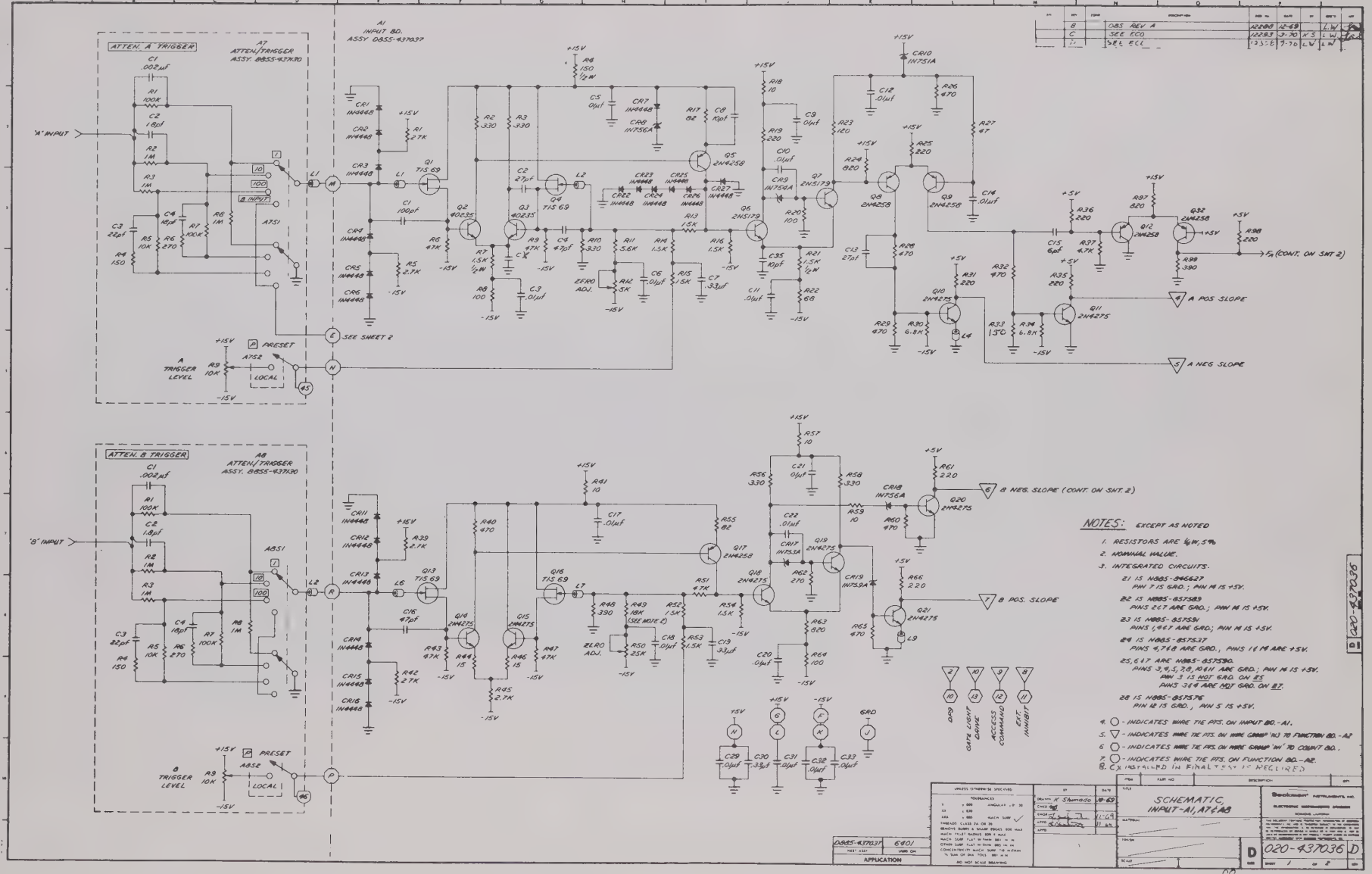
*"DM15. . . . WV4CR" are Electromotive capacitors.

**"A. B." are Allen Bradley, fixed composition resistors.

INPUT BOARD ASSEMBLY (A1) - PARTS LIST - continued

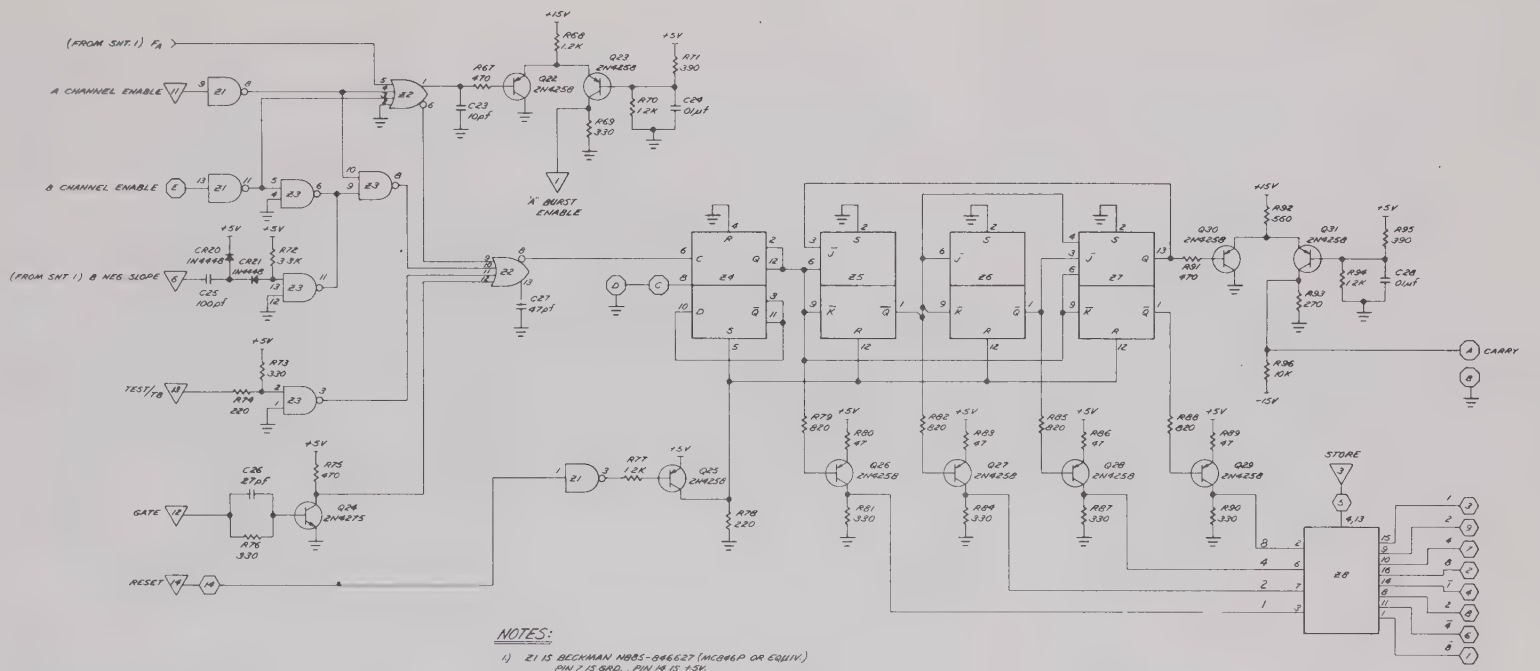
Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty./ Assy.
R12	614-841197	Resistor, Variable, 5K, 1/8W, 20%	CTS Type X-201	1
R13, 14, 15, 16, 52, 53, 54	601-822527	Resistor, 1.5K, 1/4W, 5%	*A. B. CB1525	7
R17, 55	601-822375	Resistor, 82Ω, 1/4W, 5%	A. B. CB8205	2
R18, 41, 57, 59	601-823379	Resistor, 10Ω, 1/4W, 5%	A. B. CB1005	4
R19, 25, 31, 35, 36, 61, 66, 74, 78, 98	601-822327	Resistor, 220Ω, 1/4W, 5%	A. B. CB2215	10
R22	601-823389	Resistor, 68Ω, 1/4W, 5%	A. B. CB6805	1
R23	601-823390	Resistor, 120Ω, 1/4W, 5%	A. B. CB1215	1
R24, 63, 79, 82, 85, 88, 97	601-822306	Resistor, 820Ω, 1/4W, 5%	A. B. CB8215	7
R26, 28, 29, 32, 40, 60, 65, 67, 75, 91	601-823395	Resistor, 470Ω, 1/4W, 5%	A. B. CB4715	10
R27, 80, 83, 86, 89	601-823387	Resistor, 47Ω, 1/4W, 5%	A. B. CB4705	5
R30, 34	601-822299	Resistor, 6.8K, 1/4W, 5%	A. B. CB6825	2
R33	601-823391	Resistor, 150Ω, 1/4W, 5%	A. B. CB1515	1
R37, 51	601-822297	Resistor, 4.7K, 1/4W, 5%	A. B. CB4725	2
R44, 46	601-823381	Resistor, 15Ω, 1/4W, 5%	A. B. CB1505	2
R48, 71, 95, 99	601-822371	Resistor, 390Ω, 1/4W, 5%	A. B. CB3915	4
R49	601-822303	Resistor, 18K, 1/4W, 5%	A. B. CB1835	1
R50	614-864261	Resistor, Variable, 25K, 1/8W, 20%	CTS Type X-201	1
R62, 93	601-823393	Resistor, 270Ω, 1/4W, 5%	A. B. CB2715	2
R68, 70, 77, 94	601-822326	Resistor, 1.2K, 1/4W, 5%	A. B. CB1225	4
R72	601-822296	Resistor, 3.3K, 1/4W, 5%	A. B. CB3325	1
R92	601-823396	Resistor, 560Ω, 1/4W, 5%	A. B. CB5615	1
R96	601-822324	Resistor, 10K, 1/4W, 5%	A. B. CB1035	1
XZ1 thru XZ7	860-857545	Socket, I. C., 14-Pin Dual In-Line	Cinch Mfg. Co. 133-51-02-003	7
XZ8	860-857544	Socket, I. C., 16-Pin Dual In-Line	Cinch Mfg. Co. 51-02-006	1
Z1	885-846627	I. C., MC846P	Motorola	1
Z2	885-857589	I. C., MC1023P, or equivalent	Motorola	1
Z3	885-857591	I. C., MC1010P, or equivalent	Motorola	1
Z4	885-857537	I. C., MC1034P	Motorola	1
Z5, 6, 7	885-857590	I. C., MC1013P, or equivalent	Motorola	3
Z8	885-857576	I. C., SN7475N, or equivalent	Texas Instruments	1
W1	039-437283	Wire List, 'W1' Wire Group	Beckman	1
W3	039-437285	Wire List, 'W3' Wire Group	Beckman	1

*"A. B." are Allen Bradley, fixed composition, resistors.



NOTES: EXCEPT AS NOTED

1. RESISTORS ARE ¼W, 5%
2. NOMINAL VALUE.
3. INTEGRATED CIRCUITS.
   - 21 IS N083-946627 PIN 7 IS GRD.; PIN 14 IS +5V.
   - 22 IS N085-857589 PINS 2&7 ARE GRD.; PIN 14 IS +5V.
   - 23 IS N085-857559 PINS 1,9&7 ARE GRD.; PIN 14 IS +5V.
   - 24 IS N085-857537 PINS 4,7&8 ARE GRD., PINS 1&14 ARE +5V.
   - 25,6,7 ARE N085-857590. PINS 3,9,5,7,8,10&11 ARE GRD.; PIN 14 IS +5V. PIN 3 IS NOT GRD. ON #5 PINS 3&8 ARE NOT GRD. ON #7.
   - 28 IS N085-857576 PIN 12 IS GRD., PIN 5 IS +5V.
4. ○ - INDICATES WIRE TIE PTS. ON INPUT BD.-A1.
5. ▽ - INDICATES WIRE TIE PTS. ON WIRE GROUP 'W3' TO FUNCTION BD.-A2
6. ○ - INDICATES WIRE TIE PTS. ON WIRE GROUP 'W' TO COUNT BD.
7. ○ - INDICATES WIRE TIE PTS. ON FUNCTION BD.-A2.
8. CX INSTALLED IN FINAL TEST IF NECESSARY.



NOTES:

1) Z1 IS BECKMAN N885-8946627 (MC846P OR EQUIV.)
PIN 7 IS GRD., PIN 14 IS +5V.

2) Z2 IS BECKMAN N885 8575589 (MC1023P OR EQUIV.).
PIN 7 IS GRD., PIN 14 IS +5V

3) Z3 IS BECKMAN N885-8575591 (MC1010P OR EQUIV.).
PIN 7 IS GRD., PIN 14 IS +5V

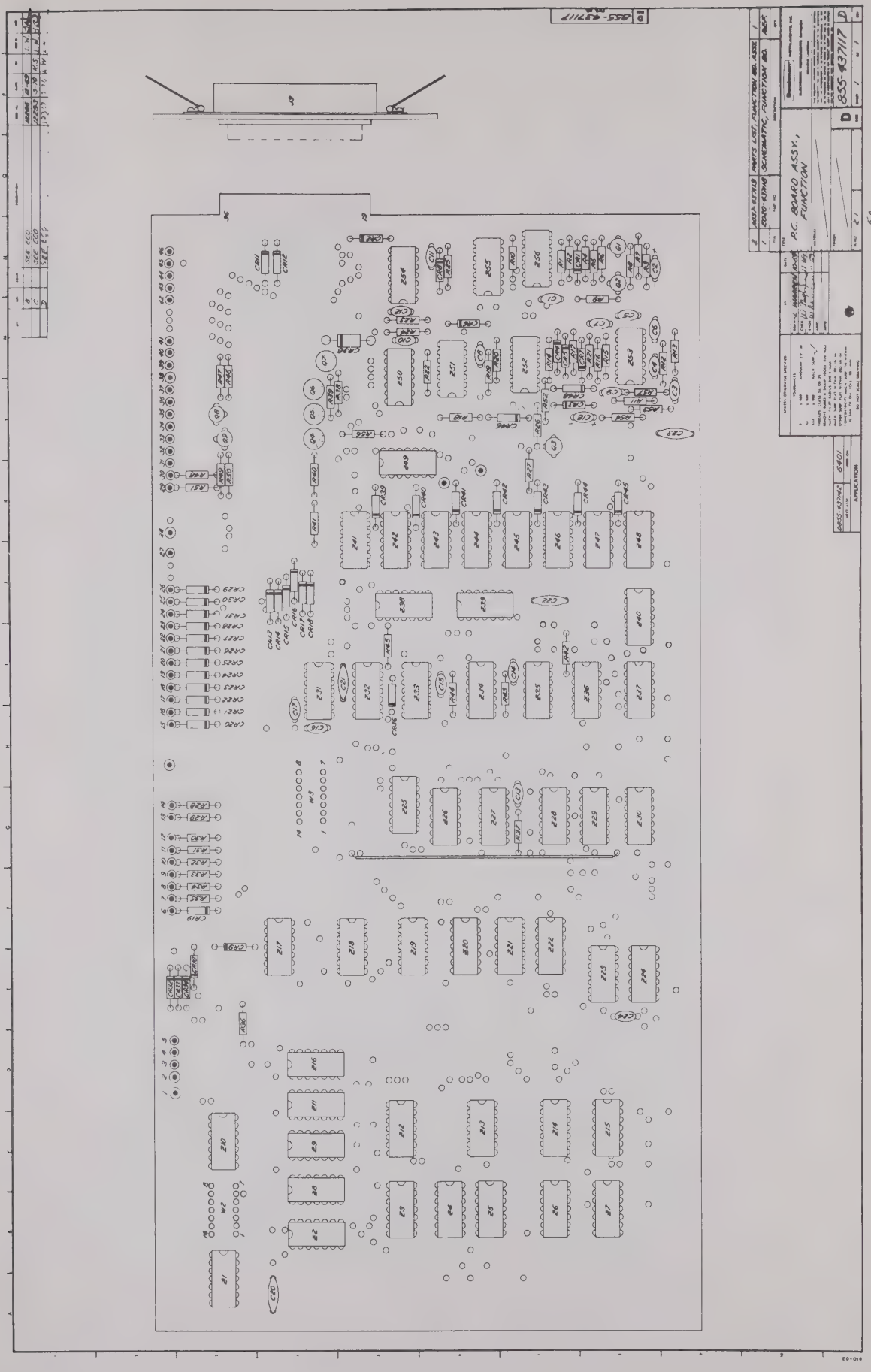
4) Z4 IS BECKMAN N885 8575537 (MC1034P OR EQUIV.).
PIN 7 IS GRD., PIN 14 IS +5V.

5) Z5, Z6, Z7 ARE BECKMAN N885-8575590 (MC1013P OR EQUIV.)
PIN 7 IS GRD., PIN 14 IS +5V ; ALL UNUSED INPUTS GROUNDED

6) Z8 IS BECKMAN N885-8575576 (SN7475 OR EQUIV.).
PIN 12 IS GRD., PIN 5 IS +5V

SCHEMATIC, INPUT-A1, AT&A3

D 020-437036 D



FUNCTION BOARD ASSEMBLY (A2) - PARTS LIST

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty. / Assy.
	D-437117-D	Function Board Assembly	Beckman	
C1, 15	637-826136	Capacitor, 120pf, 500V, 5%	*DM15F121J0-500WV4CR	2
C2, 18	631-857569	Capacitor, 33μf, 15V, 20%	Sprague 196D336X0015FB	2
C3	637-822973	Capacitor, 68pf, 500V, 5%	DM15E680J0-500WV4CR	1
C4	637-837854	Capacitor, 240pf, 500V, 5%	DM15F241J0-500WV4CR	1
C5	633-857080	Capacitor, 3300pf, 500V, 20%	Sprague 19C404A	1
C6, 8	637-822251	Capacitor, 100pf, 500V, 5%	DM15F101J0-500WV4CR	2
C7, 11, 12, 24	633-836864	Capacitor, 0.01μf, 100V	Sprague C023B101F103M	4
C9	633-846738	Capacitor, 0.02μf, 50V, 20%	Sprague 55C21A2	1
C10, 16, 17	637-822908	Capacitor, 330pf, 500V, 5%	DM15F331J0-500WV4CR	3
C13, 14	637-822771	Capacitor, 82pf, 500V, 5%	DM15E820J0-500WV4CR	2
C20, 21, 22, 23	633-815873	Capacitor, 0.33μf, 25V	Sprague 5C023334D8250B3	4
CR1 thru 31, 36,39 thru 46, 48	755-838731	Diode, 1N4448	Continental Devices	41
CR32, 33, 34	755-420893	Diode, Special	Beckman	3
CR38	755-416842	Diode, Special	Beckman	1
J9	672-824764	Connector, 36 Contact	Amphenol 57-40360	1
Q1	755-845089	Transistor, 2N4258	Fairchild	1
Q2, 3, 8, 9	755-857274	Transistor, 2N4275	Fairchild	4
Q4, 5, 6, 7	755-839888	Transistor, 2N3638A	Fairchild	4
R1, 2, 15, 16, 19, 20, 23, 24	601-822299	Resistor, 6.8K, 1/4W, 5%	**A.B. CB6825	8
R3, 11	601-822297	Resistor, 4.7K, 1/4W, 5%	A.B. CB4725	2
R4, 9, 10, 18, 22, 36	601-822308	Resistor, 1K, 1/4W, 5%	A.B. CB1025	6
R5	601-822296	Resistor, 3.3K, 1/4W, 5%	A.B. CB3325	1
R6	601-822460	Resistor, 3.9K, 1/4W, 5%	A.B. CB3925	1
R7	601-823384	Resistor, 27Ω, 1/4W, 5%	A.B. CB2705	1
R8	601-823912	Resistor, 470K, 1/4W, 5%	A.B. CB4745	1
R12, 13, 46, 49	601-823395	Resistor, 470Ω, 1/4W, 5%	A.B. CB4715	4
R14, 17, 21, 25, 52	601-822324	Resistor, 10K, 1/4W, 5%	A.B. CB1035	5
R26	601-822544	Resistor, 1.8K, 1/4W, 5%	A.B. CB1825	1
R27, 42	601-822369	Resistor, 680Ω, 1/4W, 5%	A.B. CB6815	2
R28 thru 35, 45	601-823379	Resistor, 10Ω, 1/4W, 5%	A.B. CB1005	9

continued. . .

* "DM15...." are Electromotive capacitors.

** "A.B." are Allen Bradley, fixed composition resistors.

FUNCTION BOARD ASSEMBLY (A2) - PARTS LIST - continued

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty./ Assy.
R37, 43, 44	601-823393	Resistor, 270Ω, 1/4W, 5%	*A. B. CB2715	3
R38, 39, 40, 41, 48, 51	601-822295	Resistor, 2.7K, 1/4W, 5%	A. B. CB2725	6
R47, 50, 53	601-823396	Resistor, 560Ω, 1/4W, 5%	A. B. CB5615	3
R54	601-822527	Resistor, 1.5K, 1/4W, 5%	A. B. CB1525	1
R56	601-822327	Resistor, 220Ω, 1/4W, 5%	A. B. CB2215	1
R57	601-823391	Resistor, 150Ω, 1/4W, 5%	A. B. CB1515	1
XZ1 thru XZ56	860-857545	I. C., Socket, 14 Position	Cinch 133-51-02-003	56
Z1, 10	885-857580	I. C., MC889P, or equivalent	Motorola	2
Z2, 5, 6, 7, 8, 9, 11, 15, 21, 23, 38, 39, 50, 56	885-846627	I. C., MC846P	Motorola	14
Z3, 12, 22, 24 30, 52, 54	885-846628	I. C., MC837P	Motorola	7
Z4, 13, 19	885-846625	I. C., MC826P	Motorola	3
Z14, 16, 20	885-857618	I. C., SN15849, or equivalent	Texas Instruments	3
Z17, 18, 40	885-846631	I. C., MC830P	Motorola	3
Z25, 26, 27, 29, 55	885-863951	I. C., SN7410N, or equivalent	Texas Instruments	5
Z28, 32, 37	885-846972	I. C., SN7400N, or equivalent	Texas Instruments	3
Z31	885-857538	I. C., SN7402N	Texas Instruments	1
Z33	885-857584	I. C., SN74H10N, or equivalent	Texas Instruments	1
Z34	885-857453	I. C., SN74H20N, or equivalent	Texas Instruments	1
Z35, 36	885-857575	I. C., SN7430N	Texas Instruments	2
Z41	885-857579	I. C., SN3374N, or equivalent	Texas Instruments	1
Z42 thru Z48	885-857577	I. C., SN7490N, or equivalent	Texas Instruments	7
Z49	885-857555	I. C., SN7450N	Texas Instruments	1
Z51	885-857585	I. C., SN7420N, or equivalent	Texas Instruments	1
Z53	885-857593	I. C., SN74H00N, or equivalent	Texas Instruments	1

*"A. B." are Allen Bradley, fixed composition resistors.

NOTES: FUNCTION BOARD (A2) SCHEMATIC DIAGRAM

(Part of Dwg. No. E437118)

Function Board Notes:

1) Resistors: 1/4W, 5%.

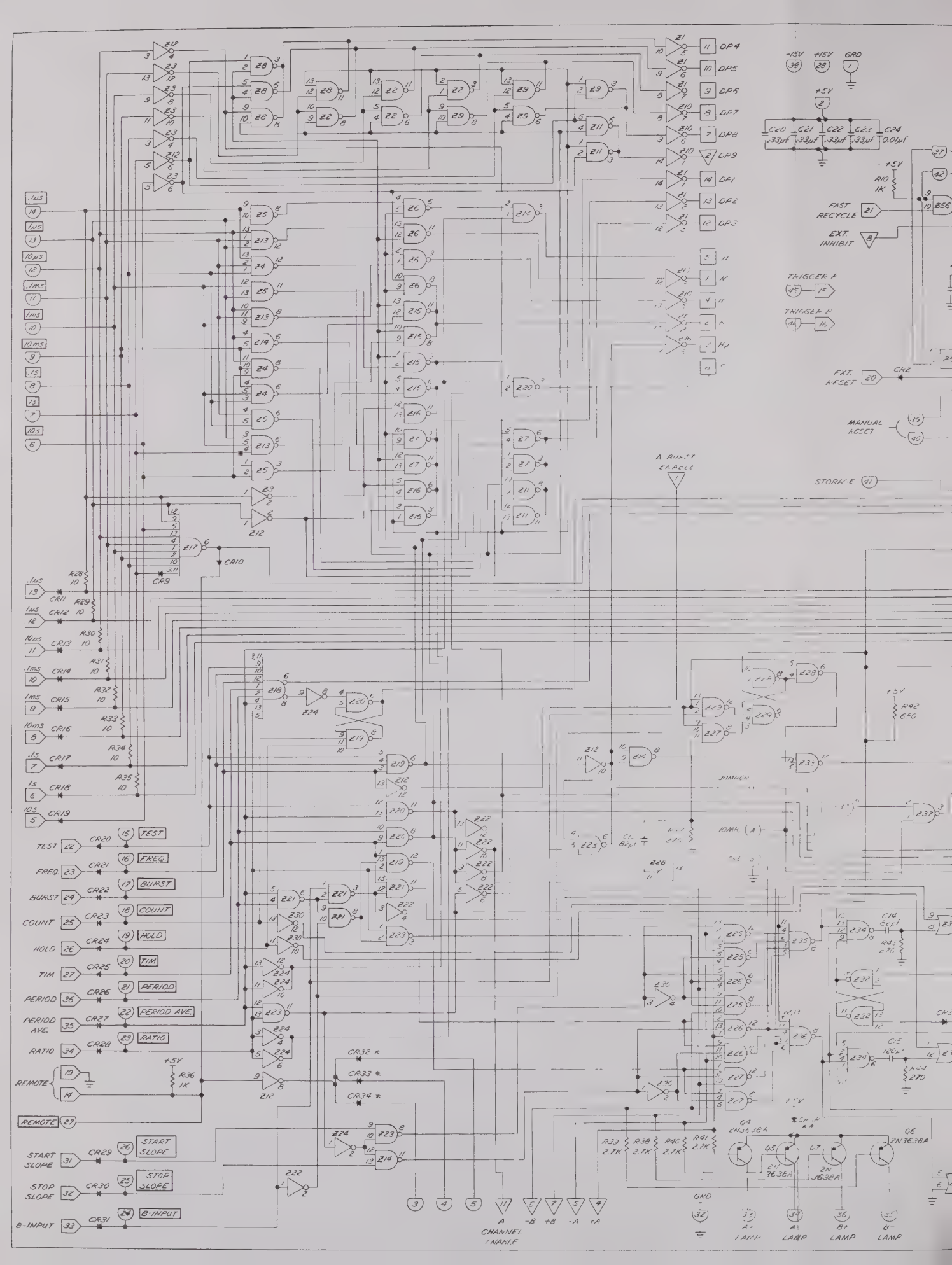
2) Board connection-point coding:
   - ⬭ Wire Connection Points.
   - ☐ Wire Group 'W2' to Count Board, A3.
   - ▽ Wire Group 'W3' to Input Board, A1.
   - ⬠ Remote Connector, J9.

3) Integrated Circuits:

Detail No.	Beckman Part No.	Typical Manufacturer No.	Gnd.	+5 V (Vcc)
	D-010-437144-D	Function Board (A2) Schematic Notes		
Z1, 10	885-857580	MC889P or equivalent	Pin 4	Pin 11
Z2, 5, 6, 7, 8, 9, 11, 15, 21, 23, 38, 39, 50, 56	885-846627	MC846P or equivalent	Pin 7	Pin 14
Z3, 12, 22, 24, 30, 52, 54	885-846628	MC837P or equivalent	Pin 7	Pin 14
Z4, 13, 19	885-846625	MC862P or equivalent	Pin 7	Pin 14
Z14, 16, 20	885-857618	SN15849 or equivalent	Pin 7	Pin 14
Z17, 18, 40	885-846631	MC830P or equivalent	Pin 7	Pin 14
Z25, 26, 27, 29, 55	885-863951	SN7410N or equivalent	Pin 7	Pin 14
Z28, 32, 37	885-846972	SN7400N or equivalent	Pin 7	Pin 14
Z31	885-857538	SN7402N or equivalent	Pin 7	Pin 14
Z33	885-857584	SN74H10N or equivalent	Pin 7	Pin 14
Z34	885-857453	SN74H20N or equivalent	Pin 7	Pin 14
Z35, 36	885-435224	SN7430N or equivalent	Pin 7	Pin 14
Z41	885-857579	SN3374N or equivalent	Pin 10	Pin 5
Z42, 43, 44, 45 46, 47, 48	885-857577	SN7490N or equivalent	Pin 10	Pin 5
Z49	885-857555	SN7450N or equivalent	Pin 7	Pin 14
Z51	885-857585	SN7420N or equivalent	Pin 7	Pin 14
Z53	885-857593	SN74H00N or equivalent	Pin 7	Pin 14

4) Diodes are 1N4448 unless noted.

* Diodes are Beckman A755-420893.
** Diodes are Beckman B755-416842.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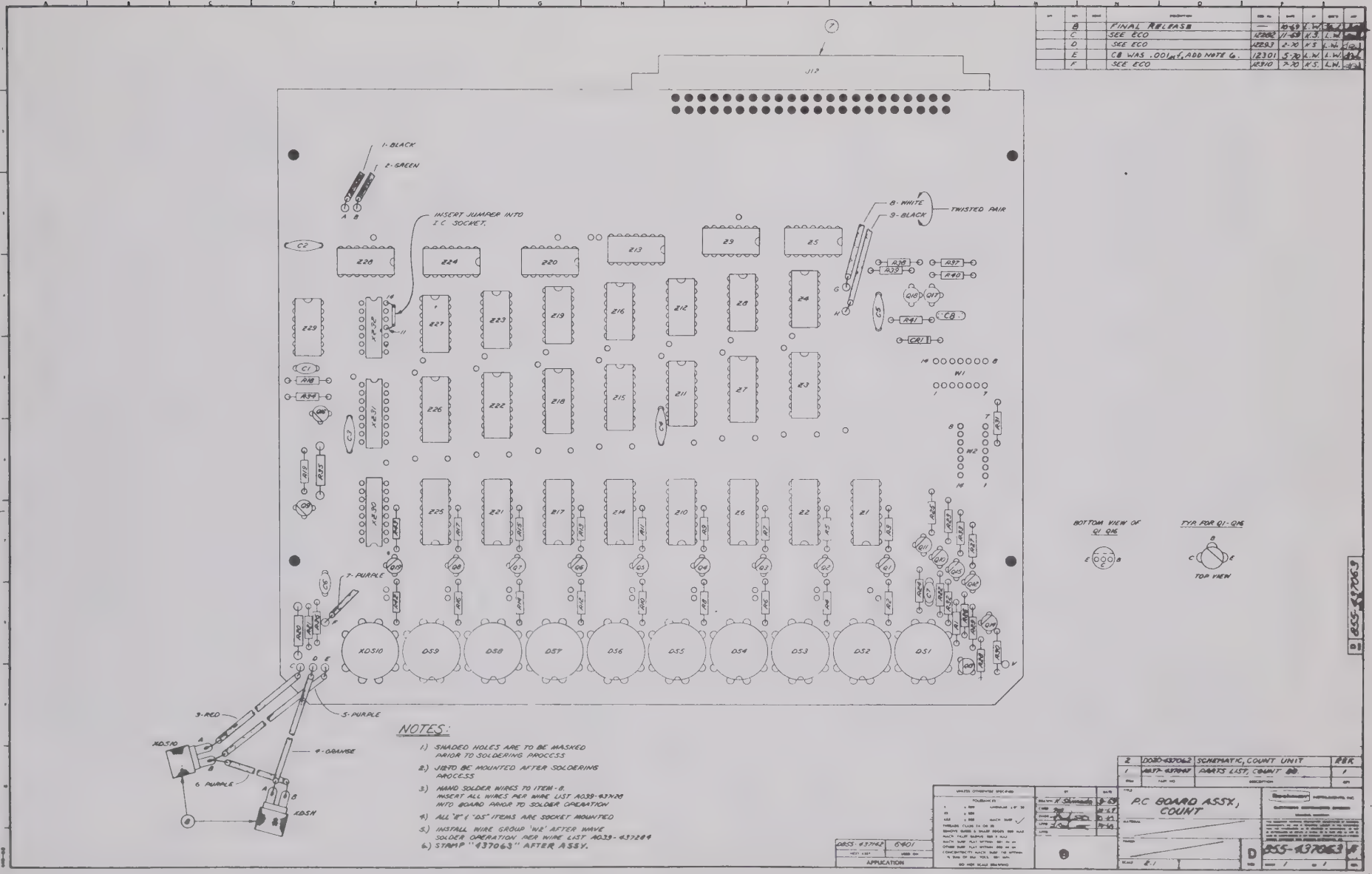
1us
10us
.1ms
1ms
10ms
.1s
1s
10s
TEST
FREQ.
BURST
COUNT
HOLD
TIM
PERIOD
PERIOD AVE.
RATIO
REMOTE
START SLOPE
STOP SLOPE
B-INPUT
DP4
DP5
DP6
DP7
DP8
DP9
DP1
DP2
DP3
-15V
+15V
GRD
+5V
FAST RECYCLE
EXT. INHIBIT
TRIGGER A
TRIGGER B
EXT. RESET
MANUAL RESET
A BURST ENABLE
STORAGE
JUMPER
A CHANNEL INHIBIT
-B
+B
-A
+A
A LAMP
B LAMP
A- LAMP
B- LAMP

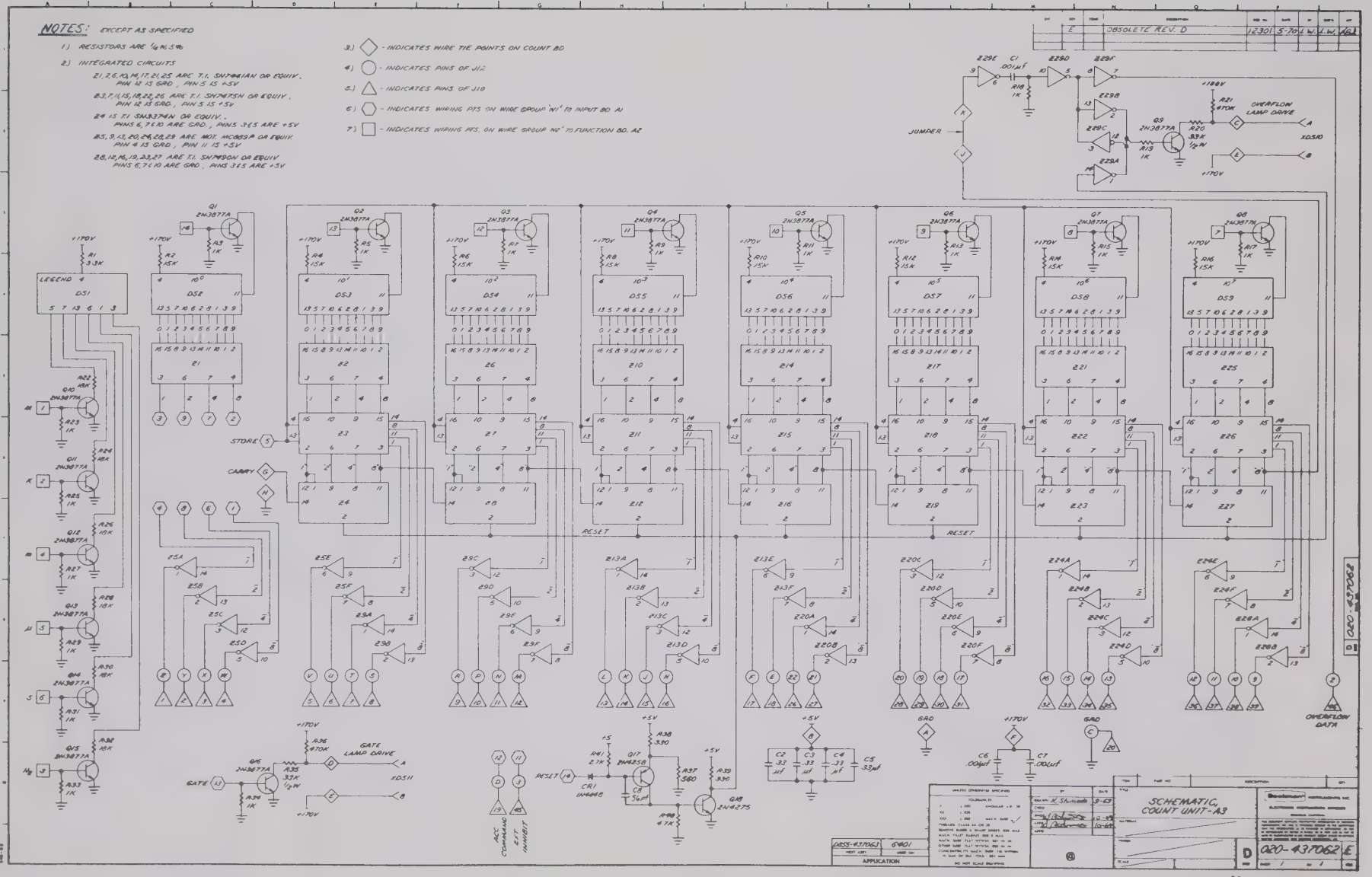

1- BLACK
2- GREEN
INSERT JUMPER INTO I C SOCKET.
8- WHITE
9- BLACK
TWISTED PAIR
7- PURPLE
3- RED
5- PURPLE
4- ORANGE
6- PURPLE
XDS10
XDS9
BOTTOM VIEW OF Q1-Q16
TYP FOR Q1-Q16
TOP VIEW
NOTES:
1.) SHADED HOLES ARE TO BE MASKED PRIOR TO SOLDERING PROCESS
2.) J1&T0 BE MOUNTED AFTER SOLDERING PROCESS
3.) HAND SOLDER WIRES TO ITEM - 8. INSERT ALL WIRES PER WIRE LIST A039-637X09 INTO BOARD PRIOR TO SOLDER OPERATION
4.) ALL "8" & "DS" ITEMS ARE SOCKET MOUNTED
5.) INSTALL WIRE GROUP 'W2' AFTER WAVE SOLDER OPERATION PER WIRE LIST A039-637209
6.) STAMP "637063" AFTER ASSY.
P.C BOARD ASSY, COUNT
DSS-637063

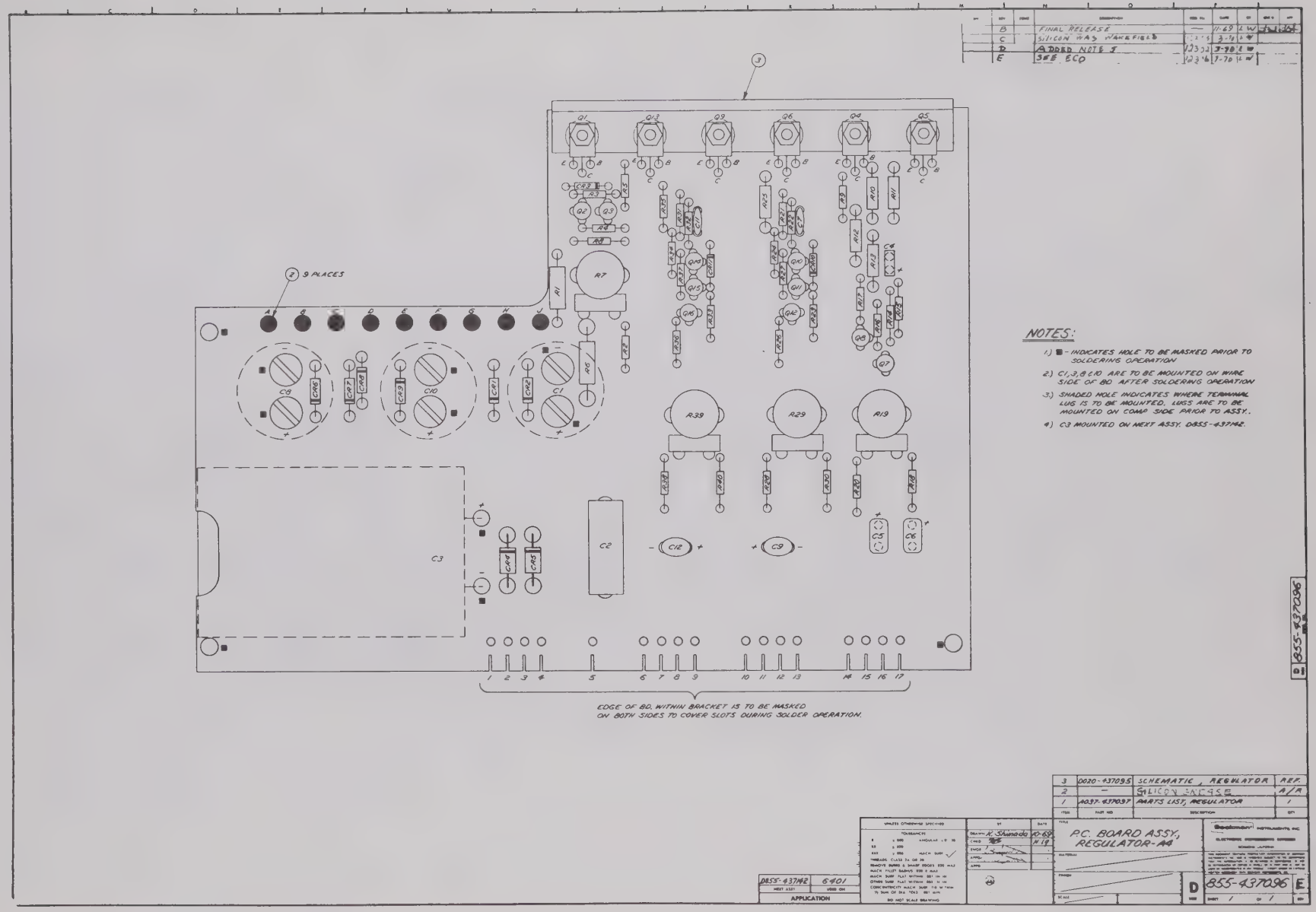
COUNT BOARD ASSEMBLY (A3) - PARTS LIST

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty./ Assy.
	D-437063-F	Count Board (A3)	Beckman	
C1, 6, 7	633-804706	Capacitor, F. Cerm., 0.001μf, 1KV, ±10%	Centralab DD-102	3
C2, 3, 4, 5	633-815873	Capacitor, F. Cerm., 0.33μf, 25V, ±20%	Sprague 5C023334-D8250B3	4
C8	637-822770	Capacitor, Dip. Mica, 56pf, 500V	Electrmtv. DM15E560J0	1
CR1	755-838731	Diode, 1N4448	Continental Devices	1
DS1	751-857284	Readout Tube, Legend	Nat'l Eltrn's. NL-867	1
DS2 thru DS9	751-857285	Readout Tube, Numerical	Nat'l Eltrn's. NL-842	8
J12	680-857546	Connector, 22 Double R/O	Amphenol 225-22221-105	1
Q1 thru Q16, 19	755-846287	Transistor, 2N3877A	G.E.	17
Q17	755-845089	Transistor, 2N4258	Fairchild	1
Q18	755-857274	Transistor, 2N4275	Fairchild	1
R1	601-822296	Resistor, 3.3K, 1/4W, 5%	*A.B. CB3325	1
R2, 4, 6, 8, 10, 12, 14, 16, 42	601-822301	Resistor, 15K, 1/4W, 5%	A.B. CB1535	9
R3, 5, 7, 9, 11, 13, 15, 17, 18, 19, 23, 25, 27, 29, 31, 33, 34, 43	601-822308	Resistor, 1K, 1/4W, 5%	A.B. CB1025	18
R20, 35	601-015060	Resistor, 33K, 1/2W, 5%	A.B. EB3335	2
R21, 36	601-823912	Resistor, 470K, 1/4W, 5%	A.B. CB4745	2
R22, 24, 26, 28, 30, 32	601-822303	Resistor, 18K, 1/4W, 5%	A.B. CB1835	6
R37	601-823396	Resistor, 560Ω, 1/4W, 5%	A.B. CB5615	1
R38, 39	601-823394	Resistor, 330Ω, 1/4W, 5%	A.B. CB3315	2
R40	601-822297	Resistor, 4.7K, 1/4W, 5%	A.B. CB4725	1
R41	601-822295	Resistor, 2.7K, 1/4W, 5%	A.B. CB2735	1
XDS1 thru 10	860-857331	Socket, Readout	Nat'l RTS-29	10
XDS10, 11	824-846653	Socket, Lamp	Eldema Q082-2K	2
XZ1, 2, 3, 6, 7, 10, 11, 14, 15, 17, 18, 21, 22, 25, 26	860-857544	Socket, I.C., 16-Pin Dual Inline	Cinch Mfg. Co. 133-51-02-006	15
XZ4, 5, 8, 9, 12, 13, 16, 19, 20, 23, 24, 27, 28, 29	860-857545	Socket, I.C., 14-Pin Dual Inline	Cinch Mfg. Co. 133-51-02-003	14
Z1, 2, 6, 10, 14, 17, 21, 25	885-857578	I.C., BCD-to-Decimal Decoder, SN7441AN	Texas Instruments	8
Z3, 7, 11, 15, 18, 22, 26	885-857576	I.C., Quadruple Bistable Latch, SN7475N	Texas Instruments	7
Z4	885-857579	I.C., Decade Counter/25 MHz, SN3374N	Texas Instruments	1
Z5, 9, 13, 20, 24, 28, 29	885-857580	I.C., Hex Inverter MC889P	Motorola	7
Z8, 12, 16, 19, 23, 27	885-857577	I.C., Decade Counter/10 MHz, SN7490N	Texas Instruments	6
W2	039-437284	Wire List, 'W2' Wire Group	Beckman	1

*"A.B." are Allen Bradley, fixed composition resistors.

Note: BCD Brd. (A6) takes connector: Beckman Part No. 672-814649; Amphenol 57-40500.


NOTES: EXCEPT AS SPECIFIED
1) RESISTORS ARE 1/4 W, 5%
2) INTEGRATED CIRCUITS
21, 26, 10, 14, 17, 21, 25 ARE T.I. SN7441AN OR EQUIV. PIN 16 IS GND, PIN 5 IS +5V
23, 7, 11, 15, 18, 22, 25 ARE T.I. SN7475N OR EQUIV. PIN 16 IS GND, PIN 5 IS +5V
24 IS T.I. SN53374N OR EQUIV., PINS 6, 7 & 10 ARE GND., PINS 3 & 5 ARE +5V
25, 9, 13, 20, 24, 28, 29 ARE MOT. MC889P OR EQUIV. PIN 4 IS GND, PIN 11 IS +5V
28, 12, 16, 19, 23, 27 ARE T.I. SN7490N OR EQUIV. PINS 5, 7 & 10 ARE GND, PINS 3 & 5 ARE +5V
3) ◇ - INDICATES WIRE TIE POINTS ON COUNT BD.
4) ○ - INDICATES PINS OF J12
5) △ - INDICATES PINS OF J10
6) ⬡ - INDICATES WIRING PTS. ON WIRE GROUP 'W1' TO INPUT BD. A1
7) □ - INDICATES WIRING PTS. ON WIRE GROUP 'W2' TO FUNCTION BD. A2
E OBSOLETE REV. D 12301 5-70
JUMPER
+170V
+188V
OVERFLOW LAMP DRIVE
OVERFLOW DATA
LEGEND
STORE
CARRY
RESET
GATE
GATE LAMP DRIVE
ACC COMMAND
EFT INHIBIT
SCHEMATIC, COUNT UNIT-A3
020-437062 E
DASS-437062 6401
APPLICATION


B FINAL RELEASE 1-69 L.W.
C SILICON WAS WAFER FIELD 2-70 L.W.
D ADDED NOTE 3 3-70 L.W.
E 3RD ECO 7-70 L.W.
3
2 9 PLACES
A1 B C D E F G H J
Q1 Q13 Q2 Q6 Q4 Q5
Q2 Q3 Q14 Q15 Q16 Q11 Q12 Q8 Q7
R7 R39 R29 R19
C9 C10 C1 C3 C2 C12 C9 C5 C6
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
EDGE OF BD. WITHIN BRACKET IS TO BE MASKED ON BOTH SIDES TO COVER SLOTS DURING SOLDER OPERATION.
NOTES:
1.) ■ - INDICATES HOLE TO BE MASKED PRIOR TO SOLDERING OPERATION
2.) C1,3,8 & 10 ARE TO BE MOUNTED ON WIRE SIDE OF BD AFTER SOLDERING OPERATION
3.) SHADED HOLE INDICATES WHERE TERMINAL LUG IS TO BE MOUNTED. LUGS ARE TO BE MOUNTED ON COMP SIDE PRIOR TO ASSY.
4.) C3 MOUNTED ON NEXT ASSY. 0855-437142.
D 855-437096
3 0020-437095 SCHEMATIC, REGULATOR REF.
2 — SILICON WAFER A/A
1 A037-437097 PARTS LIST, REGULATOR 1
DRAWN K. Shimada 10-69
CHKD N.H. 10-69
ENGR
APPD
P.C. BOARD ASSY, REGULATOR-A4
Beckman INSTRUMENTS, INC.
D 855-437096 E
SCALE
SHEET 1 OF 1
0855-437142 6401
NEXT ASSY USED ON
APPLICATION

REGULATOR BOARD (A4) - PARTS LIST

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty. / Assy.
	D855-437096-E	Regulator Board (A4)	Beckman	
C1	631-857554	Capacitor, Elect., 95μf, 350V	*36D950F350AA-2A	1
C2	641-859091	Capacitor, 0.1μf, 400V, 10%	Cornel D DPMS-4P1	1
C3	631-857552	Capacitor, Elect., 0.028f, 10V	*36D283G010BB-2A	1
C4	631-857567	Capacitor, Elect., 4.7μf, 25V, 20%	Kemet K4R7W25	1
C5, 6	631-857307	Capacitor, Elect., 250μf, 6V, 20%	Components, Inc. TSD5-6-257	2
C7, 11	633-836864	Capacitor, F. Cerm., 0.01μf, 100V	*C023B101F103M	2
C8, 10	631-857304	Capacitor, Elect., 2700μf, 25V	*36D272G025AA2B	2
C9, 12	631-857569	Capacitor, Elect., 33μf, 15V, 20%	*196D336X0015FB	2
CR1, 2, 6, 7, 8, 9	755-416842	Diode, Special	Beckman	6
CR3	755-857550	Diode, Zener, 75V, 1W, 10%, 1N4761	Motorola	1
CR4, 5	755-857551	Diode, 1N5198	Semtech	2
CR10, 11	755-818496	Diode, 5.1V, 5%, 1N751A	Motorola	2
Q1	755-866485	Transistor, 2N5195	Motorola	1
Q2, 3, 7, 8, 11, 12, 14	755-839888	Transistor, 2N3638A	Fairchild	7
Q4, 5, 9	755-862086	Transistor, 2N5193	Motorola	3
Q6, 13	755-862085	Transistor, 2N5190	Motorola	2
Q10, 15, 16	755-838784	Transistor, 2N3565	Fairchild	3
R1	601-800049	Resistor, 220Ω, 1W, 5%	**A.B. GB2215	1
R2	601-822301	Resistor, 15K, 1/4W, 5%	A.B. CB1535	1
R3	601-823397	Resistor, 5.6K, 1/4W, 5%	A.B. CB5625	1
R4	601-822297	Resistor, 4.7K, 1/4W, 5%	A.B. CB4725	1
R5, 23, 33	601-822308	Resistor, 1K, 1/4W, 5%	A.B. CB1025	3
R6	601-800068	Resistor, 56K, 1W, 5%	A.B. GB5635	1
R7	614-836291	Resistor, Var., 1K, 1/8W, 30%	CTS U-201	1
R8	607-821614	Resistor, F. Film, 6.19K, 1/4W, 1%	IRC CEB-T0	1
R9, 21, 31	601-822296	Resistor, 3.3K, 1/4W, 5%	A.B. CB3325	3
R10, 11, 13	601-022946	Resistor, 10Ω, 1/2W, 5%	A.B. EB1005	3
R12	601-800005	Resistor, 22Ω, 1/2W, 5%	A.B. EB2205	1
R14	607-826634	Resistor, F. Film, 1.21K, 1/4W, 1%	IRC CEB-T0	1
R15	607-833110	Resistor, F. Film, 249Ω, 1/4W, 1%	IRC CEB-T0	1
R16, 22, 32	601-822527	Resistor, 1.5K, 1/4W, 5%	A.B. CB1525	3
R17, 27, 35, 37	601-823396	Resistor, 560Ω, 1/4W, 5%	A.B. CB5615	4
R18, 20	607-833764	Resistor, F. Film, 182Ω, 1/4W, 1%	IRC CEB-T0	2
R19	614-844215	Resistor, Var., 100Ω, 1/8W, 30%	CTS U-201	1
R24, 34	601-822324	Resistor, 10K, 1/4W, 5%	A.B. CB1035	2

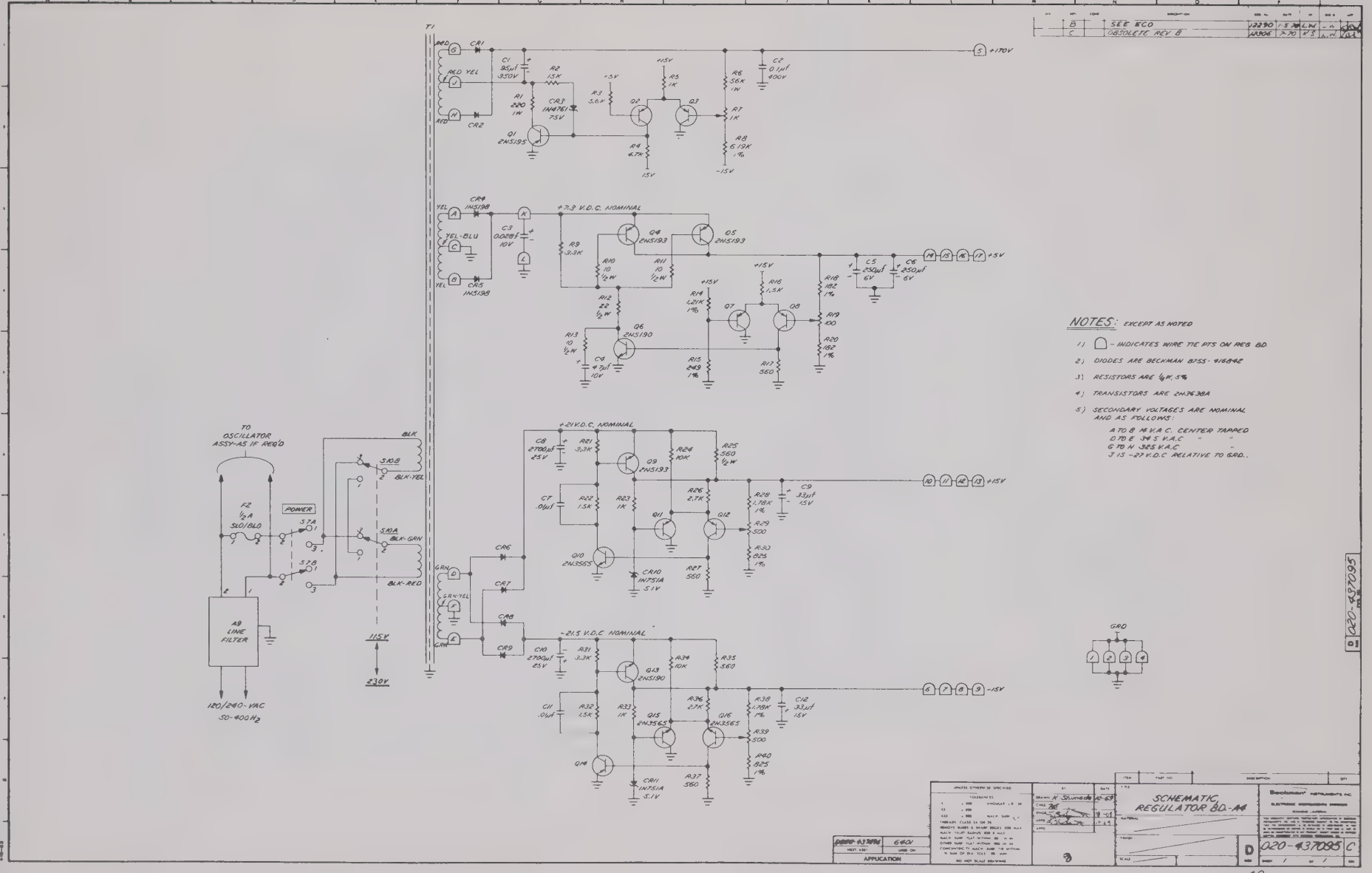
continued. . .

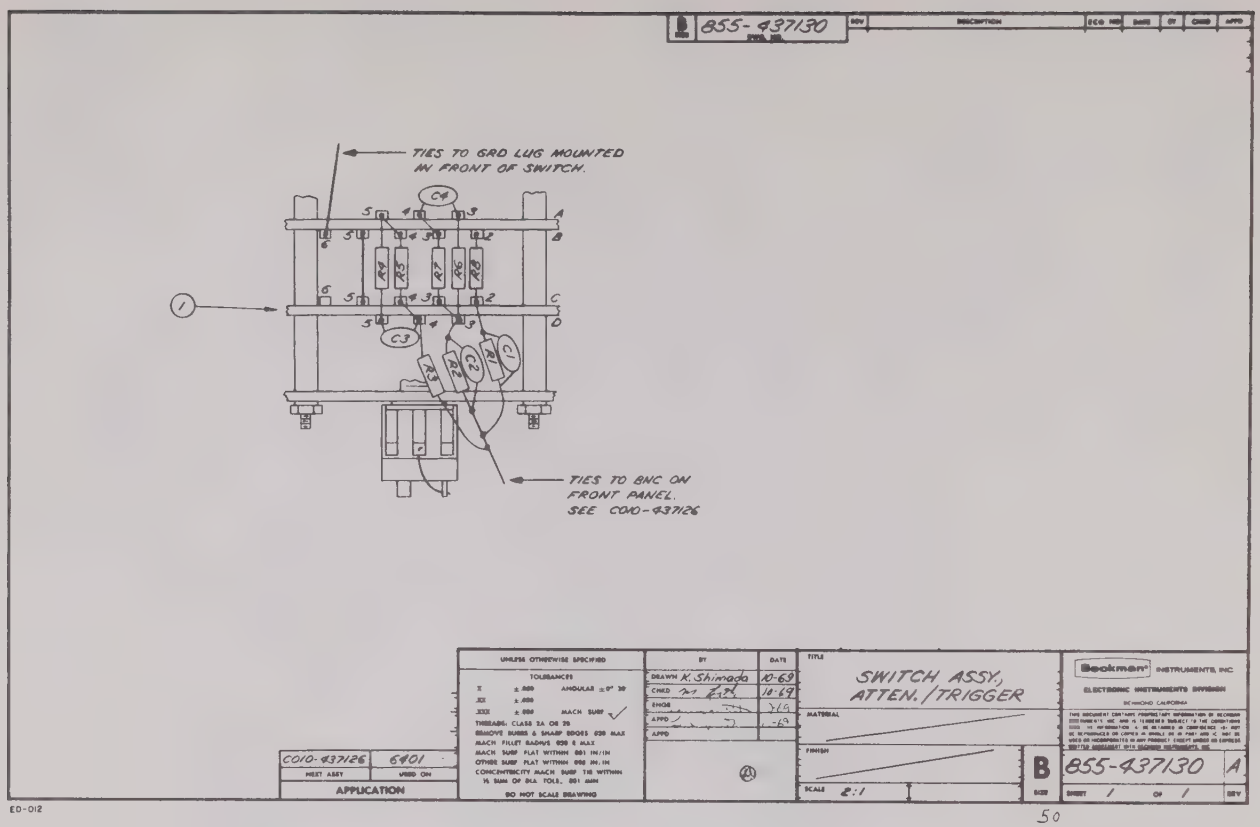
* Sprague capacitors.
** "A.B." are Allen Bradley, fixed composition, resistors.

REGULATOR BOARD (A4) - PARTS LIST - continued

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty. / Assy.
R25	601-079492	Resistor, 560Ω, 1/2W, 5%	*A.B. EB5615	1
R26,36	601-822295	Resistor, 2.7K, 1/4W, 5%	A.B. CB2725	2
R28,38	607-821612	Resistor, F. Film, 1.78K, 1/4W, 1%	IRC CEB-T0	2
R29,39	614-857557	Resistor, Var., 500Ω, 1/8W, 20%	CTS U201R501B	2
R30,40	607-822186	Resistor, F. Film, 825Ω, 1/4W, 1%	IRC CEB-T0	2
	776-437093	Heat Sink	Beckman	1

*"A.B." are Allen Bradley, fixed composition, resistors.


T1
+170V
+15V
+5V
+3.3 V.D.C. NOMINAL
+21V.D.C. NOMINAL
-21.5 V.D.C. NOMINAL
+15V
-15V
-5.1V
TO OSCILLATOR ASSY-AS IF REQ'D
A9 LINE FILTER
POWER
F2 1/2A SLO/BLO
115V
230V
120/240-VAC 50-400Hz
GRD
NOTES: EXCEPT AS NOTED
1) ⌂ - INDICATES WIRE TIE PTS ON REG BD.
2) DIODES ARE BECKMAN 8755-416842
3) RESISTORS ARE 1/4W, 5%
4) TRANSISTORS ARE 2N3638A
5) SECONDARY VOLTAGES ARE NOMINAL AND AS FOLLOWS:
A TO B 16 V.A.C. CENTER TAPPED
D TO E 34.5 V.A.C. " "
G TO N 32.5 V.A.C. " "
J TO -27 V.D.C RELATIVE TO GRD.
SEE ECO
OBSOLETE REV B
SCHEMATIC REGULATOR BD-A9
020-437095
Beckman INSTRUMENTS INC

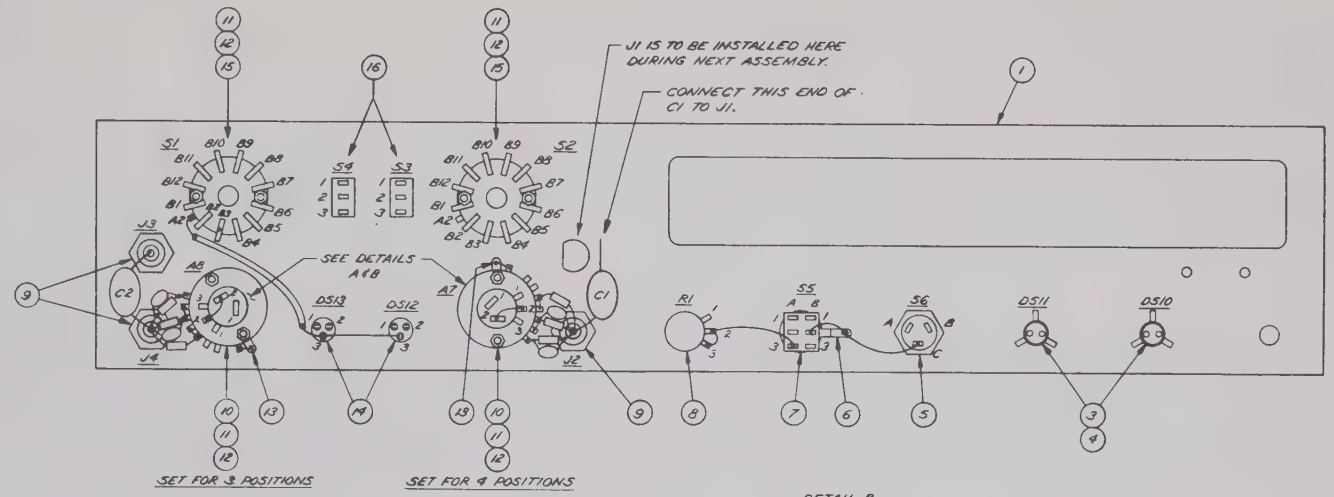


50

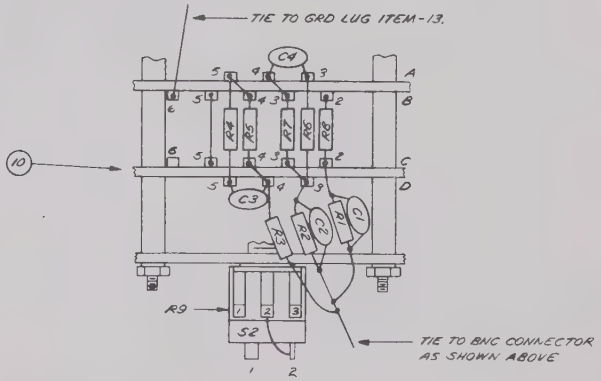
ATTEN./TRIGGER SWITCH ASSEMBLY (A7, A8) - PARTS LIST

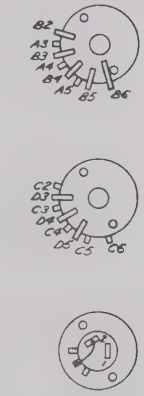
Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty./ Assy.
	B855-437130-A	Atten./Trigger Switch Assembly	Beckman	
C1	633-857033	Capacitor, 0.002μf, 600V, 5%	Skottie TXD-4-202-K	1
C2	637-857359	Capacitor, 1.8pf, 500V, 5%	Electromotive DM15-C"1.8"DO-500WV4CR	1
C3	637-832598	Capacitor, 22pf, 500V, 5%	Electromotive DM15-C220J0-500WV4CR	1
C4	637-827575	Capacitor, 18pf, 500V, 5%	Electromotive DM15C-180J0-500WV4CR	1
R1, 7	601-823904	Resistor, 100K, 1/4W, 5%	*A.B. CB1045	2
R2, 3, 8	601-823916	Resistor, 1M, 1/4W, 5%	A.B. CB1055	3
R4	601-823391	Resistor, 150Ω, 1/4W, 5%	A.B. CB1515	1
R5	601-822324	Resistor, 10K, 1/4W, 5%	A.B. CB1035	1
R6	601-823393	Resistor, 270Ω, 1/4W, 5%	A.B. CB2715	1

*"A.B." are Allen Bradley, fixed composition, resistors.


J1 IS TO BE INSTALLED HERE DURING NEXT ASSEMBLY.
CONNECT THIS END OF C1 TO J1.
SEE DETAILS A&B
SET FOR 3 POSITIONS
SET FOR 4 POSITIONS

DETAIL B
TYP. FOR A7 & A8
SCALE: 2:1





DETAIL A
TYP. FOR A7 & A8

ITEM	PART NO	DESCRIPTION	QTY
1	A037-437129	PARTS LIST, MECH & WIRED ASSY, F PANEL	REF

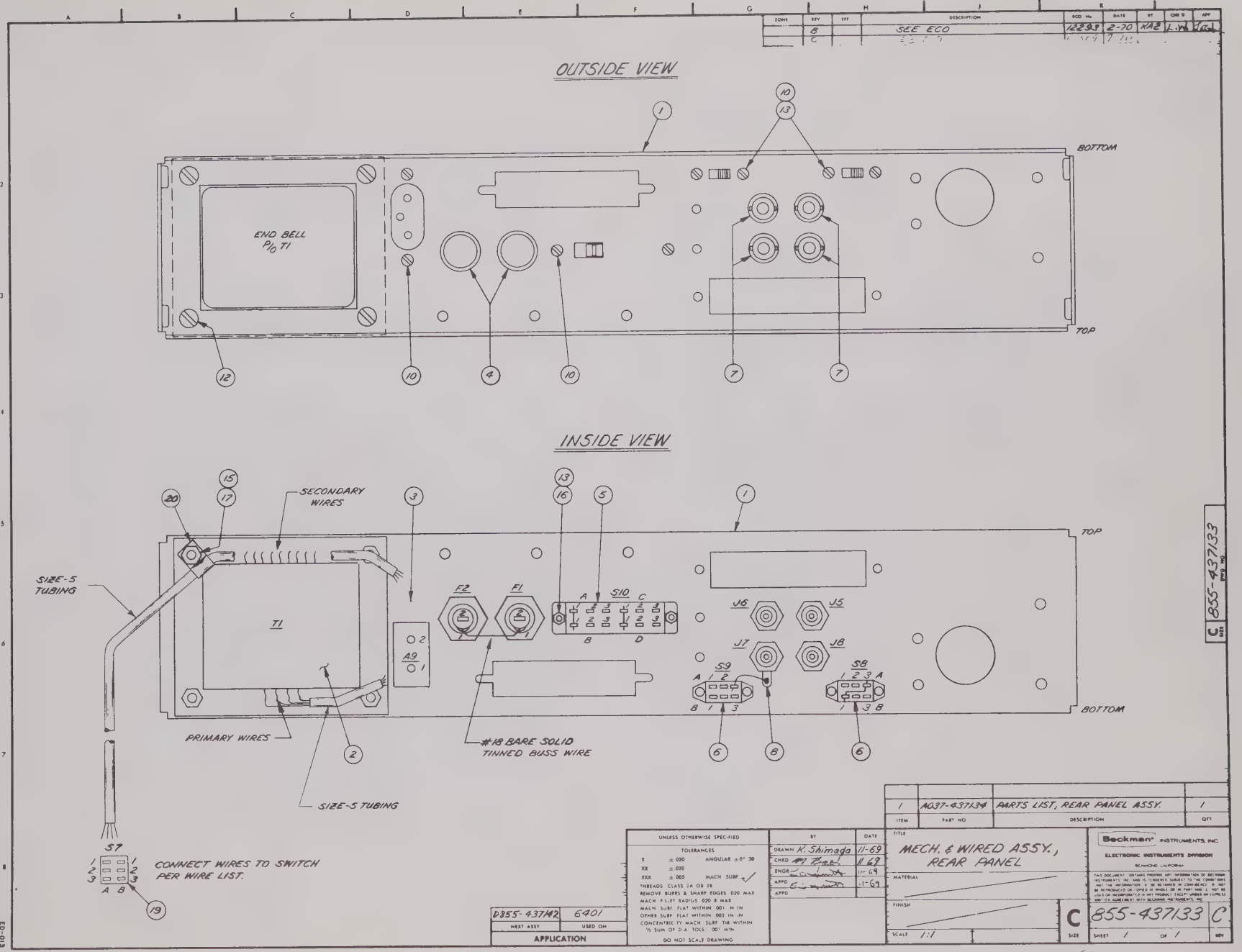
UNLESS OTHERWISE SPECIFIED
TOLERANCES
X ± .050 ANGULAR ± 0° 30'
XX ± .020
XXX ± .003 MACH SURF ✓
THREADS CLASS 2A OR 2B
REMOVE BURRS & SHARP EDGES .020 MAX
MACH FILLET RADIUS .020 R MAX
MACH SURF FLAT WITHIN .001 IN IN
OTHER SURF FLAT WITHIN .005 IN IN
CONCENTRICITY MACH SURF TIR WITHIN ½ SUM OF DIA TOLS .001 MIN
DO NOT SCALE DRAWING

	BY	DATE
DRAWN	K. Shimada	10-69
CHKD		
ENGR		
APPD		
APPD		

TITLE: MECH & WIRED ASSY, FRONT PANEL
MATERIAL:
FINISH:
SCALE: 1:1
SIZE: C
Beckman® INSTRUMENTS, INC. ELECTRONIC INSTRUMENTS DIVISION
855-437126 A
SHEET 1 OF 1

D855-437142 6401
NEXT ASSY USED ON
APPLICATION

855-437126 C



ZONE	REV	ITR	DESCRIPTION	ECO No.	DATE	BY	CHK'D	APP'D
	B		SEE ECO	12293	2-70	KAZ		
	C							

ITEM	PART NO	DESCRIPTION	QTY
1	A037-437134	PARTS LIST, REAR PANEL ASSY.	1

	BY	DATE
DRAWN	K. Shimada	11-69
CHK'D	M. Peat	11-69
ENGR		11-69
APP'D		11-69
APP'D		

UNLESS OTHERWISE SPECIFIED

TOLERANCES

X ± .050 ANGULAR ±0° 30'
XX ± .020
XXX ± .005 MACH SURF ✓

THREADS CLASS 2A OR 2B
REMOVE BURRS & SHARP EDGES .020 R MAX
MACH FILET RADIUS .020 R MAX
MACH SURF FLAT WITHIN .001 IN IN
OTHER SURF FLAT WITHIN .003 IN IN
CONCENTRIC TY MACH SURF TIR WITHIN ½ SUM OF D & TOLS .001 MIN

DO NOT SCALE DRAWING

D855-437142	6401
NEXT ASSY	USED ON
APPLICATION	

TITLE: MECH. & WIRED ASSY., REAR PANEL

MATERIAL

FINISH

SCALE 1:1

Beckman® INSTRUMENTS, INC.
ELECTRONIC INSTRUMENTS DIVISION
RICHMOND, CALIFORNIA

SIZE C | 855-437133 C | SHEET 1 OF 1 | REV

855-437133 C

FRONT PANEL MECHANICAL & WIRED ASSEMBLY - PARTS LIST

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty./ Assy.
	C-437126-A	Front Panel Mechanical & Wired Assy.	Beckman	
A7, 8	855-437130	Attenuator Switch Assembly	Beckman	2
C1, 2	633-857572	Capacitor, 0.05μf, 1KV, +100 -0%	Aerovox GPDZ5V503P	2
DS10, 11	824-846836	Lamp, Neon, Red	Eldema CG03-RCS-N12	2
DS12, 13	824-435662	Lamp Assembly	Beckman	2
J2, 3, 4	670-854373	Connector, BNC	Kings KC-79-35	3
R1	614-857570	Potentiometer, 500K, 1/4W, Linear	Mallory MLCN55L	1
S1, 2	711-437033	Switch, Rotary	Beckman	2
S3, 4	701-857324	Switch, SPDT, Toggle, w/Dress Nut	C & K 7101	2
S5	701-829909	Switch, DP3T, Toggle, w/Dress Nut	C & K 7203	1
S6	704-813496	Switch, SPDT, Pushbutton	Switchcraft 913	1
	132-824977	Clip, Lamp Mounting (use w/DS10, 11)	Eldema 081-10905	2
	662-437131	Cable Harness	Beckman	1

REAR PANEL MECHANICAL & WIRED ASSEMBLY - PARTS LIST

	C437133-C	Rear Panel Mechanical & Wired Assy.	Beckman	
A9	771-437218	Line Filter/Receptacle	Beckman	1
J5, 6, 7, 8	670-854373	Connector, BNC	Kings KC-79-35	4
S7	701-857323	Switch, DPDT, Toggle, w/Dress Nut	C & K 7201	1
S8, 9	716-827410	Switch, Slide	Continental Wirt 126	2
S10	716-857542	Switch, Slide, 115/230	Switchcraft 47227LF	1
T1	792-437140	Transformer, Power, w/Cap.	Beckman	1
XF1, 2	735-007268	Fuse Post	Bussman HKP	2

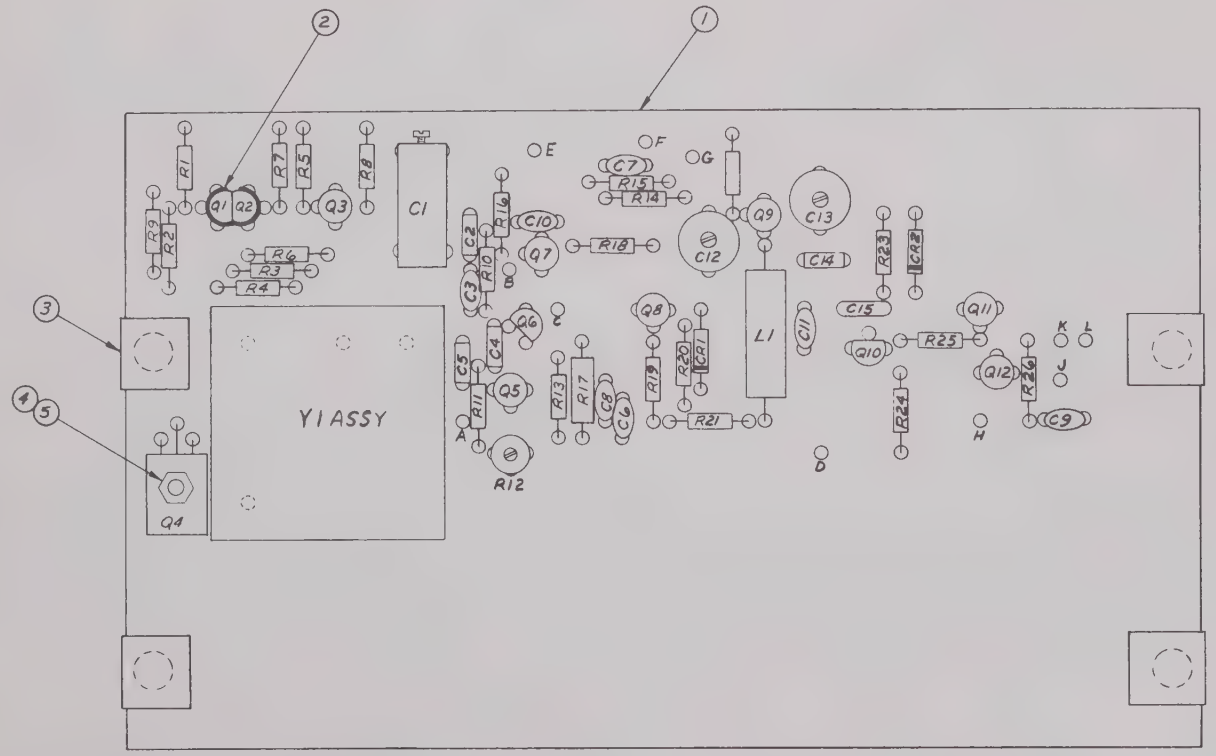
BASIC ASSEMBLY PARTS LIST

	D-437455-A	Basic Assembly	Beckman	
A6	855-437068	BCD Data Board Assembly	Beckman	1
	672-814649	Connector, 50-Pin (used with BCD Data Board)	Amphenol 57-40500	1
F2	731-092114	Fuse, 1/2A, Slo-Blo	Littelfuse 312	1
	325-437171	Knob, 1/8" Mtg., w/Dot	Raytheon	3
	325-840017	Knob, 1/4" Mtg., w/Cap.	Raytheon 257	2
	325-857549	Knob, 1/4" Mtg., Concentric	Raytheon 70 Series	2
	313-516291	Foot	Beckman	4
	327-516292	Support Mount (Tilt Foot Bail)	Beckman	1
	664-853435	Line Cord, Detachable	Belden 17258	1
	330-516285	Handle	Beckman	2
	330-526309	Handle, Grip	Beckman	2

MECHANICAL & WIRED ASSEMBLY PARTS LIST

	D-437453-A	Mechanical & Wired Assembly	Beckman	
A1	855-437037	Input Board Assembly	Beckman	1
A2	855-437117	Function Board Assembly	Beckman	1
A3	855-437063	Count Board Assembly	Beckman	1
A4	855-437096	Regulator Board Assembly	Beckman	1
J1	670-854373	Connector, BNC	Amphenol 31-221/ Astro-Plate	1
	783-807862	Ferrite Bead	Ferroxcube 56-590-65/ 3B	2

ZONE	REV	ECO	DESCRIPTION	ECO No.	DATE	BY	CHK'D	APP'D
	A		RELEASED ON ECO	12304	5-70	L.W.	L.W.	[illegible]



NOTE:
1.) INSTALL WIRES PER WIRE LIST A039-437358 AFTER SOLDER OPERATION.

ITEM	PART NO	DESCRIPTION	QTY
2	D020-437359	SCHEMATIC, OSC.	REF.
1	A037-437357	PARTS LIST, OSC. BD.	1

UNLESS OTHERWISE SPECIFIED
TOLERANCES
X ± .050 ANGULAR ± 0 30
XX ± .020
XXX ± .005 MACH SURF ✓
THREADS CLASS 2A OR 2B
REMOVE BURRS & SHARP EDGES .020 MAX
MACH FILLET RADIUS .020 R MAX
MACH SURF FLAT WITHIN .001 IN IN
OTHER SURF FLAT WITHIN .005 IN IN
CONCENTRICITY MACH SURF TO WITHIN ½ SUM OF DIA TOL.5 .001 MIN
DO NOT SCALE DRAWING

	BY	DATE
DRAWN	L. WARREN	5-70
CHKD	E. DeLOVA	5-70
ENGR		
APPD		5-72
APPD		

TITLE: ASSY, P.C. BD OSC.
MATERIAL
FINISH
SCALE
SIZE: C
SHEET OF

Beckman® INSTRUMENTS, INC.
ELECTRONIC INSTRUMENTS DIVISION

855-437355 A

0050-437457	6401-0
NEXT ASSY	USED ON
APPLICATION	

ED-013

C 855-437355 REV A

MODEL 6401-O BOARD LAYOUT (A5) PARTS LIST

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty./ Assy.
	C-437355-A	Board Layout (A5)	Beckman	
C1	655-838318	Capacitor, Var., Glass	J. F. D. VC-31GW	1
C2	633-857625	Capacitor, F. Ceramic, 12 pF, NPO	Erie 301-000C060120J	1
C3, 6, 7, 8, 9, 10, 11	633-836864	Capacitor, F. Ceramic, 0.01μF, 50V	Sprague C023B101F103M	7
C4, 5, 14	633-804660	Capacitor, F. Ceramic, 10pF, NPO	Aerovox TC-SI-1-NPO-100D	3
C12, 13	643-857510	Capacitor, Var., 5.5 to 18pF	Erie 538-011-C0P0-92R	2
C15	637-857360	Capacitor, F. Mica, 2.2pF	Electromotive DM15C"2.2"-D0500WV4CR	1
CR1, 2	755-838731	Diode, 1N4448	Continental Devices	2
L1	795-857600	Inductor, F., 10μH	Standwyck 81001M	1
Q1, 2	755-857620	Transistor, TIS97	Texas Instruments	2
Q3	755-839888	Transistor, 2N3638A	Fairchild	1
Q4	755-855012	Transistor, 2N4918	Motorola	1
Q5	755-857328	Transistor, 40235	RCA	1
Q6	755-869156	Transistor, 2N5245	Texas Instruments	1
Q7, 8, 9, 11, 12	755-857274	Transistor, 2N4275	Fairchild	5
Q10	755-857485	Transistor, TIS 58, Green	Texas Instruments	1
R1, 7	607-825323	Resistor, F. Film, 5.11K, 1/4W, 1%	IRC CEB-TO	2
R2, 4	607-825321	Resistor, F. Film, 1K, 1/4W, 1%	IRC CEB-TO	2
R3, 6	607-825879	Resistor, F. Film, 100Ω, 1/4W, 1%	IRC CEB-TO	2
R5	*601-822326	Resistor, 1.2K, 1/4W, 5%	*	1
R8	601-822299	Resistor, 6.8K, 1/4W, 5%		1
R9	601-823378	Resistor, 5.1Ω, 1/4W, 5%		1
R10	601-823912	Resistor, 470K, 1/4W, 5%		1
R11	601-823913	Resistor, 560K, 1/4W, 5%		1
R12	613-844269	Resistor, Var., Cermet, 1 Meg.	Helipot 62P R1M	1
R13	601-823397	Resistor, 5.6K, 1/4W, 5%		1
R14	601-822327	Resistor, 220Ω, 1/4W, 5%		1
R15, 20	601-822308	Resistor, 1K, 1/4W, 5%		2
R16	601-822324	Resistor, 10K, 1/4W, 5%		1
R17	601-015038	Resistor, 1K, 1/2W, 5%		1
R18	601-823391	Resistor, 150Ω, 1/4W, 5%		1

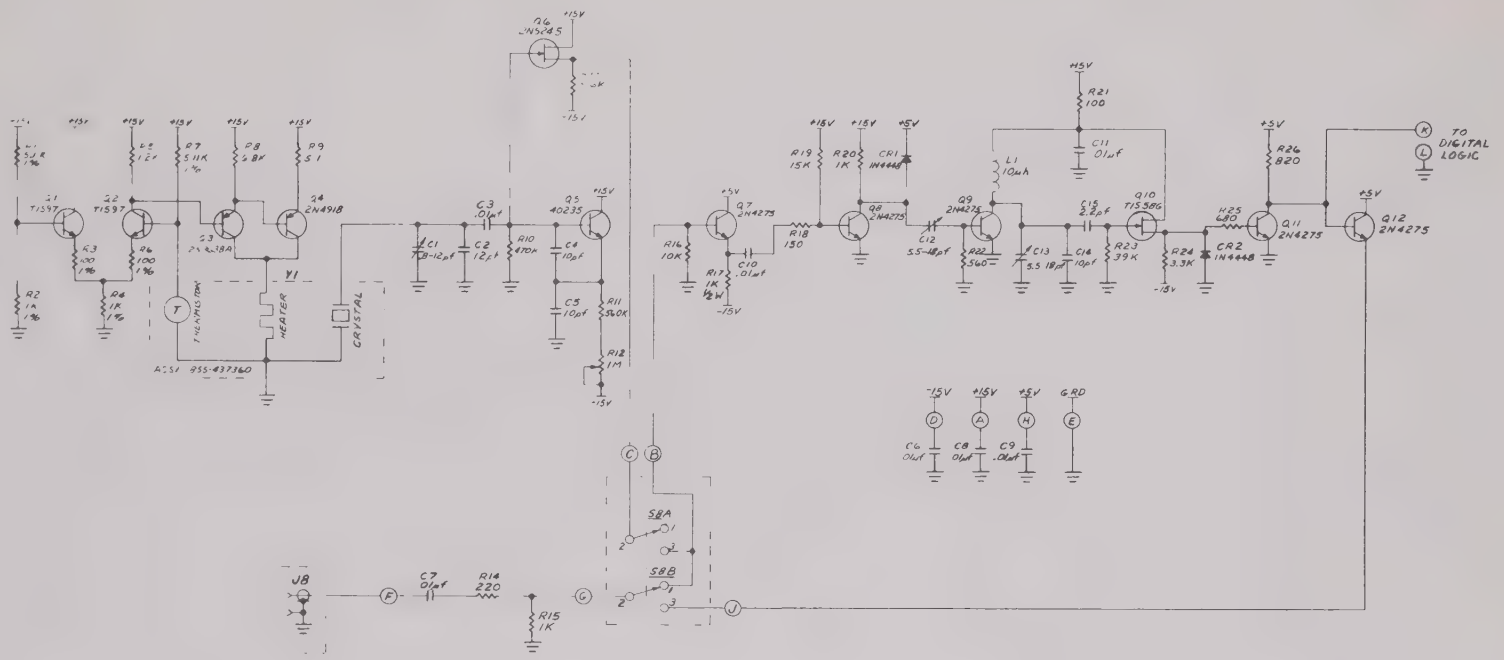
continued. . .

*Beckman Part No. prefix "601" are Allen Bradley, fixed composition resistors.

MODEL 6401-O BOARD LAYOUT (A5) PARTS LIST - continued

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty. / Assy.
R19	*601-822301	Resistor, 15K, 1/4W, 5%	*	1
R21	601-817735	Resistor, 100Ω, 1/4W, 5%		1
R22	601-823396	Resistor, 560Ω, 1/4W, 5%		1
R23	601-823901	Resistor, 39K, 1/4W, 5%		1
R24	601-822296	Resistor, 3.3K, 1/4W, 5%		1
R25	601-822369	Resistor, 680Ω, 1/4W, 5%		1
R26	601-822306	Resistor, 820Ω, 1/4W, 5%		1
Y1	855-437360	Oven Assembly	Beckman	1

*Beckman Part No. prefix "601" are Allen Bradley, fixed composition resistors.



NOTES:

1.) RESISTORS ARE ¼W, 5% UNLESS OTHERWISE SPECIFIED.
2.) C2 IS NOMINALLY 12pf.
3.) R11 IS NOMINALLY 560K.

RELEASED ON ECO 12304 5-70 LW L.W.

WARREN 5-70
L Dekan 5-70

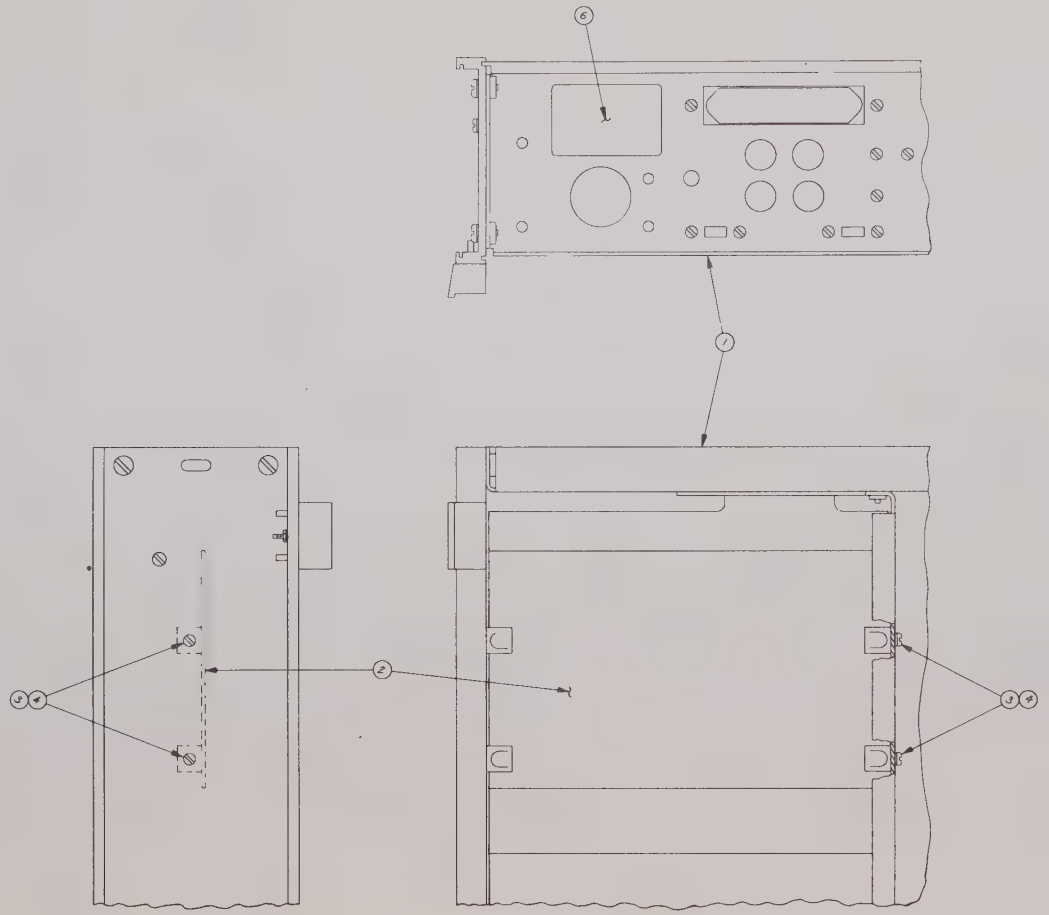
SCHEMATIC, OSCILLATOR

020-437359 A

C855-437355 G401

APPLICATION

020-437359 D1



NOTES:

1.) REMOVE BOTH REAR PANEL TRIMS
2.) REMOVE BOTTOM COVER & RIGHT DRESS PANEL
3.) INSTALL OSCILLATOR ASSEMBLY AS SHOWN AT LEFT.
4.) WIRING TO BE PER WIRE LIST A039-437358.
5.) ATTACH NAMEPLATE ON REAR PANEL AS SHOWN AT LEFT.
6.) TEST INSTRUMENT AND CABINETIZE.

ITEM	PART NO	DESCRIPTION	QTY
2	0022-437145	BLOCK DIAGRAM	REF.
1	A037-437458	PARTS LIST, FINAL ASSY, 6401-0	1

D 050-437457 REV

UNLESS OTHERWISE SPEC'D TOLERANCES
X ± .030 ANGULAR ± 0 30
XX ± .010
XXX ± .005 MACH SURF
THREADS CLASS 3A OR 3B
REMOVE BURRS & SHARP EDGES .020 MAX
MACH FILLET RADIUS .030 MAX
MACH SURF FLAT WITHIN .001 IN IN
OTHER SURF FLAT WITHIN .002 IN IN
CONCENTRICITY MACH SURF TIR WITHIN ½ SUM OF TOL .001 MIN
DO NOT SCALE DRAWING

BY DATE
DRAWN K. Shimada 7-20
CHKD 7-20
ENGR
APPD
APPD 7-20

TITLE FINAL ASSY, 6401-0
MATERIAL
FINISH
SCALE

Beckman INSTRUMENTS, INC. ELECTRONIC INSTRUMENTS DIVISION RICHMOND, CALIFORNIA

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D 050-437457 A
SHEET 1 OF 1

6401-0
NEXT ASSY USED ON
APPLICATION

SECTION 6. OPTIONS

		Page
C9 Option -	Description	1
	Count Board Assembly Modification and Parts List	2
	Schematic Diagram (B437245-A)	3
C11 Option -	Description	1
	Programmable Attenuator Board Assembly (B437228-A)	2
	AC-DC Remote Board Assembly (A437220-A)	2
	Front Panel Modification (B437241-A)	2
	Parts Lists	3
	Schematic Diagram (C437227-A)	4

C9 OPTION

DESCRIPTION

This option adds a ninth digit. The Count Board Assembly is modified as shown in Drawing No. B437246.

THEORY OF OPERATION

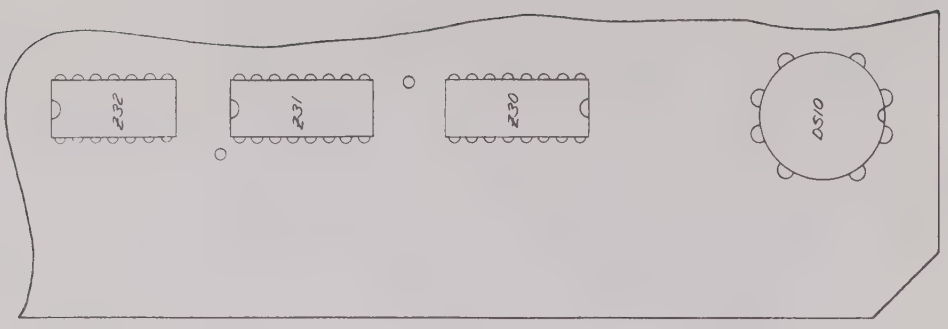
Refer to Section 3 of the Model 6401 manual.

TROUBLESHOOTING

Refer to Section 3 of the Model 6401 manual.

DIAGRAMS AND PARTS LISTS

	Dwg. No.	Page
Count Board Assembly Modification w/Parts List	B437246	2
Schematic Diagram	B437245	3

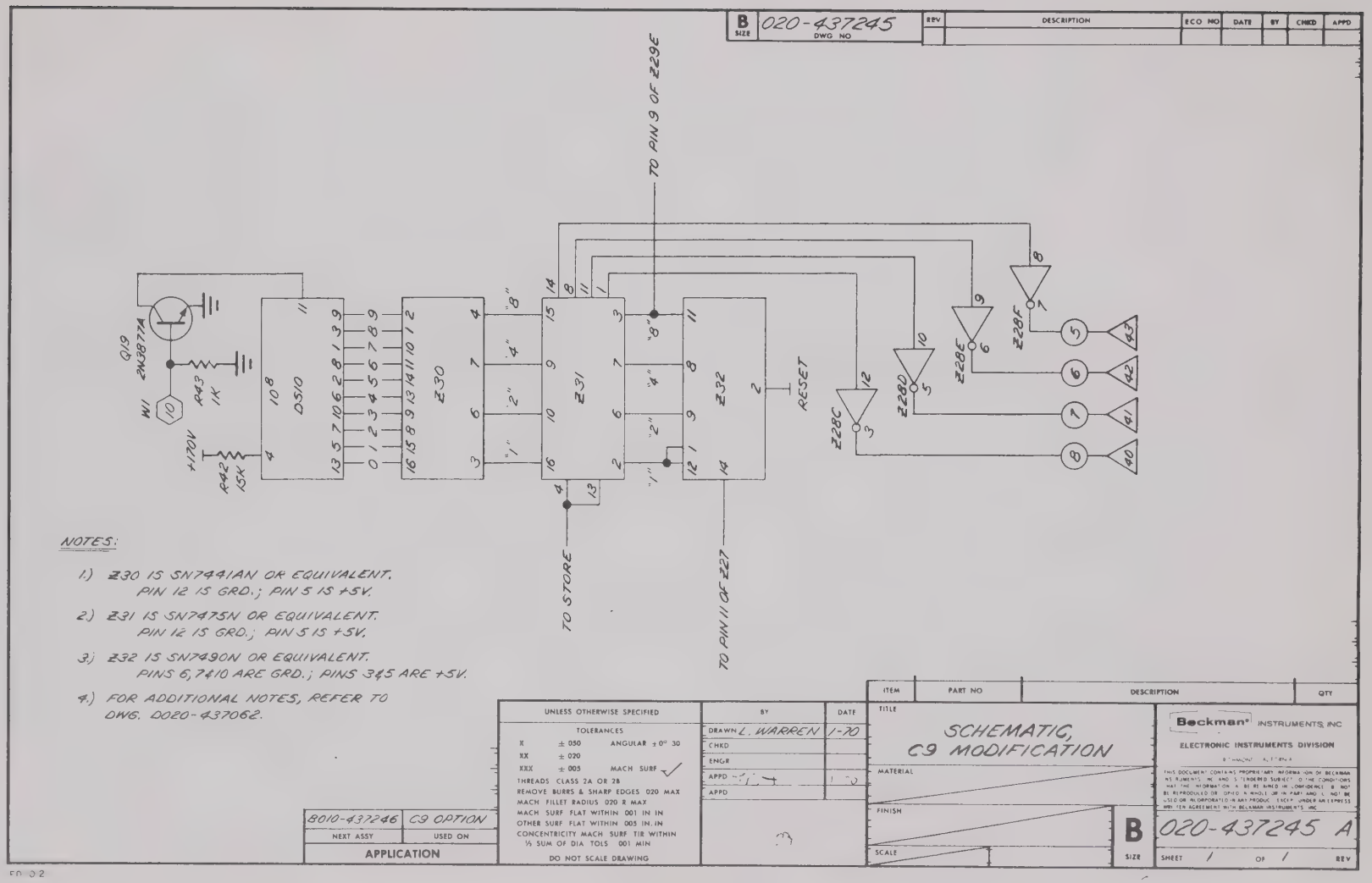


C9 OPTION
COUNT BOARD ASSEMBLY MODIFICATION

C9 Option
Model 6401
B-010-437246-B (6-70)
Beckman

C9 OPTION
COUNT BOARD ASSEMBLY PARTS LIST

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty./ Assy.
	B-437246-B	C9 Mod., Count Board Assembly	Beckman	
DS10	751-857285	Readout Tube, Numerical	Nat'l Elect. NL-842	1
Z30	885-857578	I.C., BCD-to-Decimal Decoder, SN7441AN	Tex. Instr., or equiv.	1
Z31	885-857576	I.C., Quadruple Bistable Latch, SN7475N	Tex. Instr., or equiv.	1
Z32	885-857577	I.C., Decade Counter/10 MHz, SN7490N	Tex. Instr., or equiv.	1


B SIZE
020-437245 DWG NO
REV
DESCRIPTION
ECO NO
DATE
BY
CHKD
APPD
TO PIN 9 OF Z29E
Q19 2N3877A
R43 1K
+12V
R42 15K
108
D510
Z30
Z31
Z32
RESET
Z28C
Z28D
Z28E
Z28F
"8"
"4"
"2"
"1"
TO STORE
TO PIN 11 OF Z27
NOTES:
1.) Z30 IS SN7441AN OR EQUIVALENT. PIN 12 IS GRD.; PIN 5 IS +5V.
2) Z31 IS SN7475N OR EQUIVALENT. PIN 12 IS GRD.; PIN 5 IS +5V.
3) Z32 IS SN7490N OR EQUIVALENT. PINS 6,7&10 ARE GRD.; PINS 3&5 ARE +5V.
4.) FOR ADDITIONAL NOTES, REFER TO DWG. D020-437062.
UNLESS OTHERWISE SPECIFIED
TOLERANCES
X ± 050 ANGULAR ± 0° 30
XX ± 020
XXX ± 005 MACH SURF
THREADS CLASS 2A OR 2B
REMOVE BURRS & SHARP EDGES 020 MAX
MACH FILLET RADIUS 020 R MAX
MACH SURF FLAT WITHIN 001 IN IN
OTHER SURF FLAT WITHIN 005 IN. IN
CONCENTRICITY MACH SURF TIR WITHIN ½ SUM OF DIA TOLS 001 MIN
DO NOT SCALE DRAWING
BY
DATE
DRAWN L. WARREN 1-70
CHKD
ENGR
APPD
APPD
ITEM
PART NO
DESCRIPTION
QTY
TITLE
SCHEMATIC, C9 MODIFICATION
MATERIAL
FINISH
SCALE
B SIZE
Beckman INSTRUMENTS, INC
ELECTRONIC INSTRUMENTS DIVISION
020-437245 A
SHEET 1 OF 1 REV
8010-437246 C9 OPTION
NEXT ASSY USED ON
APPLICATION

C11 OPTION

DESCRIPTION

This option adds a Programmable Attenuator and AC-DC select per channel.

THEORY OF OPERATION

The C11 option provides remote control of the input coupling, and the three attenuator positions. The option can be applied to one or both input channels.

In the local mode of operation, reed relays are controlled by front-panel switches to attenuate the input signal. In REMOTE the input signal is applied to the AC input of the channel, and a reed relay places a dc short circuit between the AC and DC input connectors. Input attenuation is accomplished by switching two form C reed relays connected to resistor capacitor networks.

TROUBLESHOOTING

Connect a signal generator to the input connector of the input channel believed to be defective. Set the frequency to approximately 1 MHz.

Monitor wire to point M for A Channel, or R for B Channel with an oscilloscope. Select X1 attenuator setting in the local mode of operation. Rotate the attenuator switch to the X10 and X100 positions and observe the wire tie point. The signal amplitude should decrease as the attenuator setting is increased.

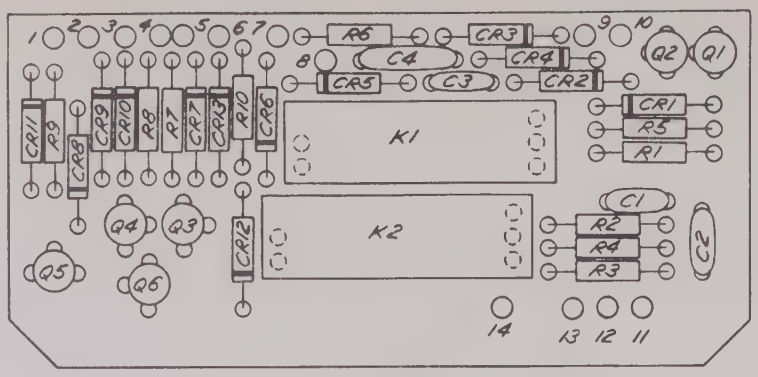
If the attenuator operates in the local mode but fails in the REMOTE mode, check the wire harness and the remote input diode for that control line.

DIAGRAMS AND PARTS LISTS

	Dwg. No.	Page
Programmable Attenuator P. C. Brd. Assy. Diagram	B437228	2
AC-DC Remote P. C. Brd. Assy. Diagram	A437220	2
Front-Panel Modification	B437241	2
Programmable Attenuator Brd. Assy. Parts List		3
AC-DC Remote P. C. Brd. Assy. Parts List		3
Schematic Diagram	C437227	4

NOTE:

DELETE C4 ON "A" ATTEN. BD. ASSY. WHEN "A" ASSY. IS USED WITH "B" ASSY. .

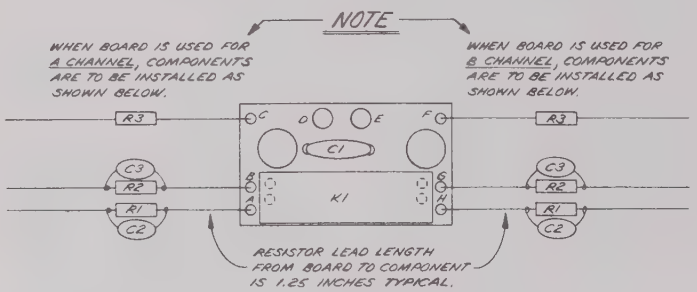


C11 OPTION

PROGRAMMABLE ATTENUATOR P.C. BOARD ASSEMBLY

C11 Option
Model 6401
B855-437228-A (8-70)

Beckman

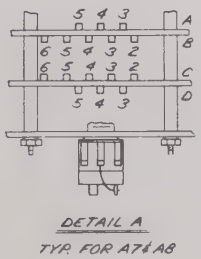


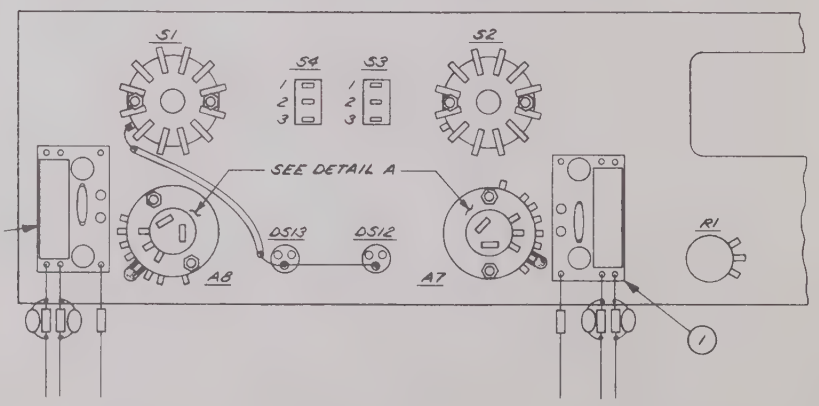
C11 OPTION

AC-DC REMOTE P.C. BOARD ASSEMBLY

C11 Option
Model 6401
A855-437220-A (8-70)

Beckman





C11 OPTION

FRONT PANEL MODIFICATION

C11 Option
Model 6401
B010-437241-A (8-70)

Beckman

C11 OPTION

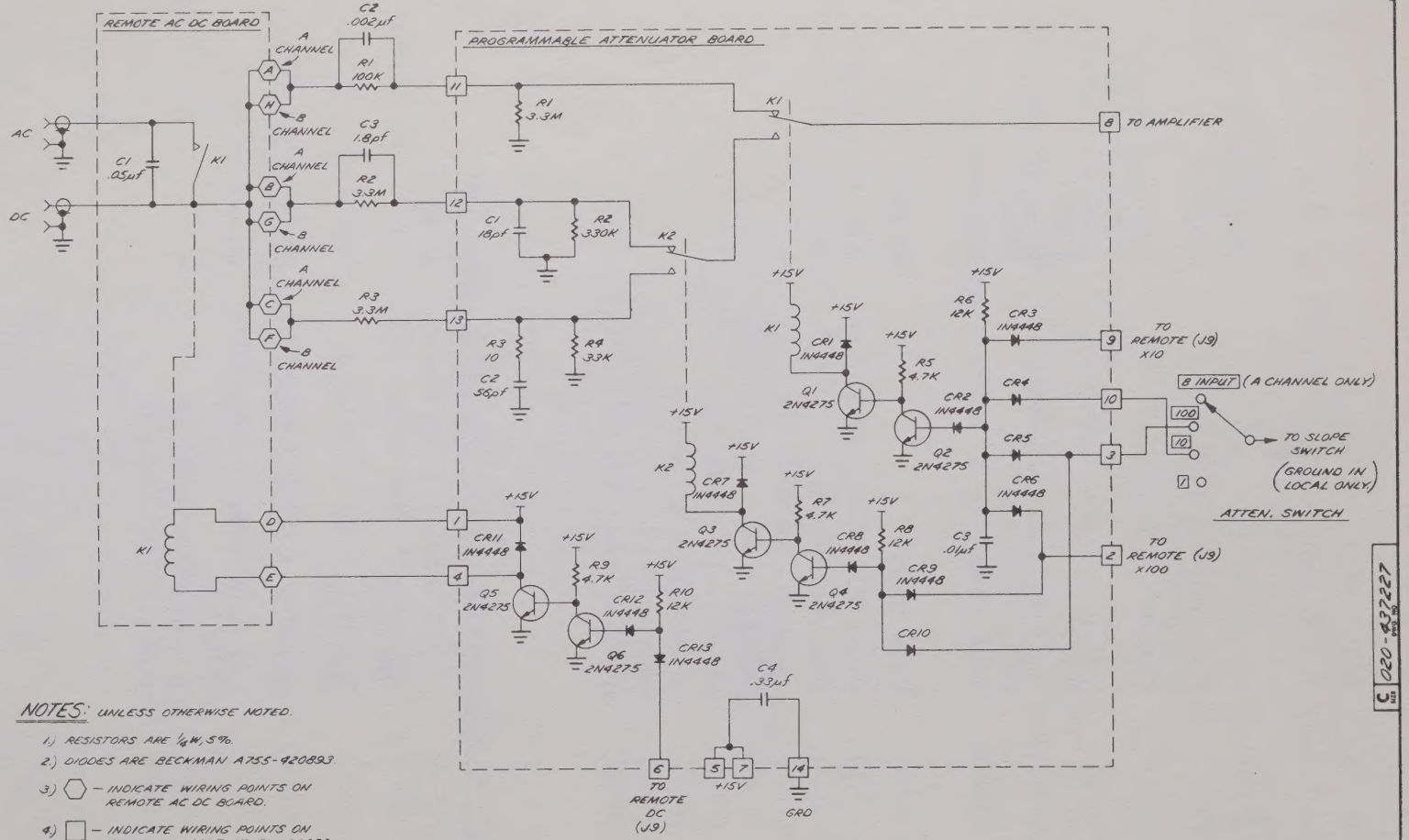
PROGRAMMABLE ATTENUATOR BOARD ASSEMBLY PARTS LIST

Detail No.	Beckman Part No.	Description	Typical Manufacturer & No.	Qty./ Assy.
	B-437228-A	Programmable Attenuator P. C. Board Assembly	Beckman	
C1	637-827575	Capacitor, F. Mica, 18pf, 500V, 5%	Electromotive DM15-C180J0-500WV4CR	1
C2	637-822770	Capacitor, F. Mica, 56pf, 500V, 20%	Electromotive DM15-E560J0	1
C3	633-836864	Capacitor, F. Cerm., 0.01μf, 100V, 20%	Sprague C023B101F-103M	1
CR1, 2, 3, 6, 7, 8, 9, 11, 12, 13	755-838731	Diode, 1N4448	Continental Devices	10
CR4, 5, 10	755-420893	Diode, Special	Beckman	3
K1, 2	718-857594	Reed Relay, Form C, 1000Ω, 12V	Jenco RR10-31-12	2
Q1, 2, 3, 4, 5, 6	755-857274	Transistor, 2N4275	Fairchild	6
R1	601-819695	Resistor, 3.3M, 1/4W, 5%	*	1
R2	601-823910	Resistor, 330K, 1/4W, 5%		1
R3	601-823379	Resistor, 10Ω, 1/4W, 5%		1
R4	601-822531	Resistor, 33K, 1/4W, 5%		1
R5, 7, 9	601-822297	Resistor, 4.7K, 1/4W, 5%		3
R6, 8, 10	601-801803	Resistor, 12K, 1/4W, 5%		3

AC-DC REMOTE P. C. BOARD ASSEMBLY PARTS LIST

	A-437220-A	AC DC Remote P. C. Board Assy.	Beckman	
C1	633-857572	Capacitor, F. Mica, 0.05μf, 1KV, +100 -000%	Aerovox GPDZ5V503P	1
C2	633-857033	Capacitor, F. Cerm., 0.002μf, 500V, 10%	Skottie TXD-4-202-K	1
C3	637-857359	Capacitor, F. Mica, 1.8pf, 500V, 5%	Electromotive DM15-C"1.8"D05WV4CR	1
K1	718-857595	Reed Relay, Form A, RR10-01-12, 1000Ω 12V	Jenco RR10-01-12	1
R1	601-823904	Resistor, 100K, 1/4W, 5%	*	1
R2, 3	601-819695	Resistor, 3.3M, 1/4W, 5%		2

* Beckman Part No. prefix "601" are Allen Bradley, fixed composition resistors.



NOTES: UNLESS OTHERWISE NOTED.

1.) RESISTORS ARE 1/4W, 5%.

2.) DIODES ARE BECKMAN A755-920893.

3.) ⬡ – INDICATE WIRING POINTS ON REMOTE AC DC BOARD.

4.) □ – INDICATE WIRING POINTS ON PROGRAMMABLE ATTEN. BOARD.

ZONE	REV	BY	DESCRIPTION	PCO No.	DATE	BY	CHK'D	APP'D

ITEM	PART NO	DESCRIPTION	QTY

UNLESS OTHERWISE SPECIFIED
TOLERANCES
X ± 030 ANGULAR ± 0 30
XX ± 010
XXX ± 005 MACH SURF ✓
THREADS CLASS 2A OR 2B
REMOVE BURRS & SHARP EDGES 020 MAX
MACH FILLET RADIUS 020 R MAX
MACH SURF FLAT WITHIN 001 IN IN
OTHER SURF FLAT WITHIN 005 IN IN
CONCENTRICITY MACH SURF TIR WITHIN
½ SUM OF DIA TOLS 001 MIN
DO NOT SCALE DRAWING

	BY	DATE
DRAWN	K. Shimada	1-70
CHK'D		
ENGR		
APP'D		
APP'D		

TITLE: SCHEMATIC, CII OPTION

Beckman® INSTRUMENTS, INC
ELECTRONIC INSTRUMENTS DIVISION

MATERIAL
FINISH
SCALE

C SIZE | 020-437227 | A REV

SHEET 1 OF 1

A955-437220	CII OPTION
B855-437228	
NEXT ASSY	USED ON
APPLICATION	

C 020-437227

Beckman

Electronic Instruments Di
3900 River Road
Schiller Park, Illinois 60
Tel: (312) 671-330(

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